CHAPTER 4. HARDWARE DESCRIPTION

1. CPU (MSM80C88A)

1-1. GENERAL DESCRIPTION

The MSM80C88A-10 are internal 16-bit CPUs with 8-bit interface implemented in Silicon Gate CMOS technology. They are designed with the same processing speed as the NMOS8086-1, but with considerably less power consumption.
The processor has attributes of both 8 and 16-bit microprocessor. It is directly compatible with MSM80C86A-10 software and MSM80C85A/MSM80C85A-2 hardware and peripherals.

1-2. FEATURES

- 8-Bit Data Bus Interface
- 16-Bit Internal Architecture
- 1 Mbyte Direct Addressable Memory Space
- Software Compatible with MSM80C86A
- Internal 14 word by 16-bit Register Set
- 24 Operand Addressing Modes
- Bit, Byte, Word and String Operations
- 8 and 16-bit Signed and Unsigned Arithmetic Operation
- From DC to 10 MHz Clock Rate
- Low Power Dissipation (10 mA/MHz)
- Bus Hold Circuitry Eliminates Pull-Up Resistors
- 56 pin(L)-V Plastic QFP (QFP56-P-910-WK)

1-3. FUNCTIONAL BLOCK DIAGRAM

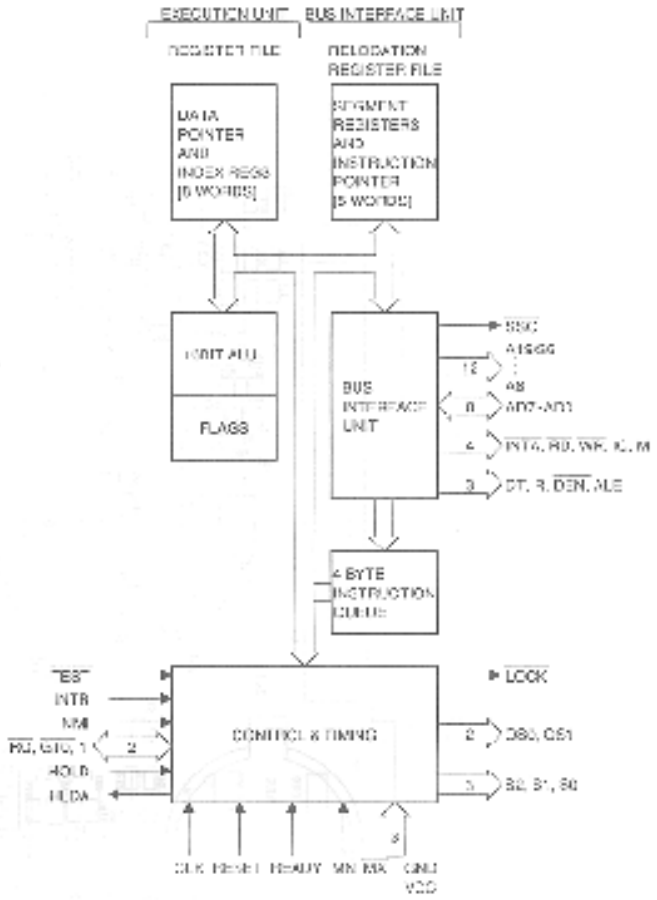


Fig.1-1 Block diagram

1-4. STATIC OPERATION

All MSM80C88A circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The MSM80C88A can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The MSM80C88A can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C86s power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the MSM80C86A power requirement is the standby current (500 µA maximum).

The BIU performs instruction fetch and queueing, operand fetch, DATA read and write address relocation and basic bus control. By performing instruction prefetch while waiting for decoding and execution of instruction, the CPU's performance is increased. Up to 4 bytes to instruction stream can be queued.
EU receives pre-fetched instructions from the BIU queue, decodes and executes instructions and provides an un-relocated operand address to the BIU.

1-5. FUNCTIONAL DESCRIPTION

(1) GENERAL OPERATION

The internal function of the M5M80C88A consist of a Bus Interface Unit (BIU) and an Execution Unit (EU). These units operate mutually but perform as separate processors.

(2) MEMORY ORGANIZATION

The M5M80C88A has a 20-bit address to memory.
Each address has 8-bit data width. Memory is organized 00000H to FFFFFH and is logically divided into four segments: code, data, extra data and stack segment.
Each segment contains up to 64 Kbytes and locates on a 16-byte boundary. (Fig. 3a)
All memory references are made relative to a segment register according to a select rule. Memory location FFFF0H is the start address after reset, and 00030H through 003FFH are reserved as an interrupt pointer. There are 256 types of interrupt pointer;
Each interrupt type has a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address.

Memory Organization

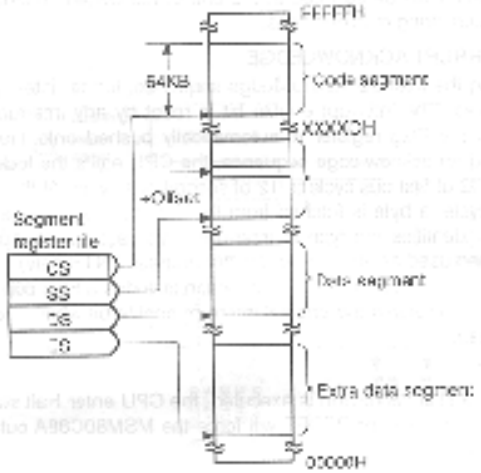


Fig.1-2 Memory organization

Reserved Memory Locations

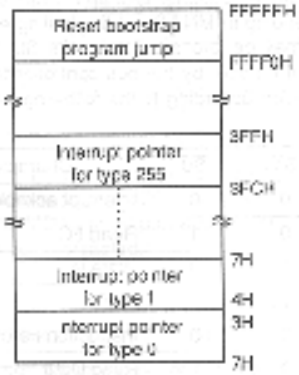


Fig.1-3 Reserved Memory Locations

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

Table 1-1. Segment selection

(3) MINIMUM AND MAXIMUM MODES

The MSM80C88A has two system modes: minimum and maximum. When using the maximum mode, it is easy to organize a multiple-CPU system with the MSM82C88 Bus Controller which generates the bus control signal.

When using the minimum mode, it is easy to organize a simple system by generating the bus control signal itself. MN/$\overline{MX}$ is the mode select pin. Definition of 24-31, 34 pin changes depends on the MN/$\overline{MX}$ pin.

(4) BUS OPERATION

The MSM80C88A has a time multiplexed address and data bus. If a non-multiplexed bus is desired for the system, it is only needed to add the address latch.

A CPU bus cycle consists of at least four clock cycles. T1, T2, T3 and T4. (See Fig.1-4)

The address output occurs during T1, and data transfer occurs during T3 and T4. T2 is used for changing the direction of the bus during read operation. When the device which is accessed by the CPU is not ready to data transfer and send to the CPU "NOT READY" is indicated TW cycles are inserted between T3 and T4.

When a bus cycle is not needed, T1 cycles are inserted between the bus cycles for internal execution.

At the T1 cycle an ALE signal is output from the CPU or the MSM82C88 depending in MN/$\overline{MX}$, at the trailing edge of an ALE, a valid address may be latched. Status bits S0, S1 and S2 are used, in maximum mode, by the bus controller to recognize the type of bus operation according to the following table. (See Table 1-2)

S2	S1	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Table 1-2. Status bits selection

Status bit S3 through S6 are multiplexed with A16 - A19, and therefore they are valid during T2 through T4. S3 and S4 indicate which segment register was selected on the bus cycle, according to the following table. (See Table 1-3)

S4	S3	Characteristics
0 (LOW)	0	Alternate Data (Extra Segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

Table 1-3 S5 indicates interrupt enable Flag

(5) I/O ADDRESSING

The MSM80C88A has a 64 Kbyte I/O. When the CPU accesses an I/O device, address A0 - A15 are in same format as a memory access, and A16 - A19 are low.

I/O ports address are same as four memory.

1-6. EXTERNAL INTERFACE

(1) RESET

CPU initialization is executed by the RESET pin.

The MSM80C88A's RESET high signal is required for greater than 4 clock cycles.

The rising edge of RESET terminates the present operation immediately. The falling edge of RESET triggers an internal reset sequence for approximately 10 clock cycles. After internal reset sequence is finished, normal operation begins from absolute location FFFF0H.

(2) INTERRUPT OPERATIONS

The interrupt operation is classified as software or hardware, and hardware interrupt is classified as nonmaskable or maskable.

An interrupt causes a new program location which is defined by the interrupt pointer table, according to the interrupt type. Absolute location 00000H through 003FFH is reserved for the interrupt pointer table. The interrupt pointer table consists of 256 elements. Each element is 4 bytes in size and corresponds to an 8-bit type number which is sent from an interrupt request device during the interrupt acknowledge cycle.

(3) NON-MASKABLE INTERRUPT (NMI)

The MSM80C88A has a non-maskable interrupt (NMI) which is of higher priority than a maskable interrupt request (INTR).

An NMI request pulse width needs minimum of 2 clock cycles. The NMI will be serviced at the end of the current instruction or between string manipulations.

(4) MASKABLE INTERRUPT (INTR)

The MSM80C88A provides another interrupt request (INTR) which can be masked by software. INTR is level triggered, so it must be held until interrupt request is acknowledged.

The INTR will be serviced at the end of the current instruction or between string manipulations.

(5) INTERRUPT ACKNOWLEDGE

During the interrupt acknowledge sequence, further interrupts are disabled. The interrupt enable bit is reset by any interrupt after which the Flag register is automatically pushed onto the stack. During an acknowledge sequence, the CPU emits the lock signal from T2 of first bus cycle to T2 of second bus cycle. At the second bus cycle a byte is fetched from the external device as a vector which identifies the type of interrupt. This vector is multiplied by four and used as an interrupt pointer address (INTR only).

The Interrupt Return (IRET) instruction includes a Flag pop operation which returns the original interrupt enable bit when it restores the Flag.

(6) HALT

When a Halt instruction is executed, the CPU enter Halt state. An interrupt request or RESET will force the MSM80C88A out of the Halt state.

(7) SYSTEM TIMING-MINIMUM MODE

A bus cycle begins at T1 with an ALE signal. The trailing edge of ALE is used to latch the address. Form T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. From T2 to T4, the address data bus changes the address bus to the data bus.

The read ($\overline{RD}$), write ($\overline{WR}$), and interrupt acknowledge ($\overline{INTA}$) signals caused the addressed device to enable the data bus. These signals become active at the beginning of T2 and inactive at the beginning of T4.

(8) SYSTEM TIMING-MAXIMUM MODE

In maximum mode the MSM82C88 Bus Controller is added to system. The CPU sends status information to the bus Controller. bus timing signals are generated by the Bus Controller. Bus timing is almost the same as in minimum mode.

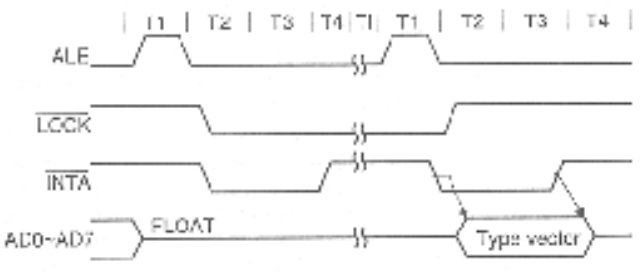


Fig.1-4 Interrupt Acknowledge Sequence

2. DVC ASIC (μPD65658)

2-1. General

The DVC is ASIC having the following functions

<CPU interface>

- CPU Bus Interface

<Memory interface>

- VRAM interface

<Device controllers>

- Serial port control (Equality with M82510B)
- Parallel port control
- LCD control

2-2. Block diagram

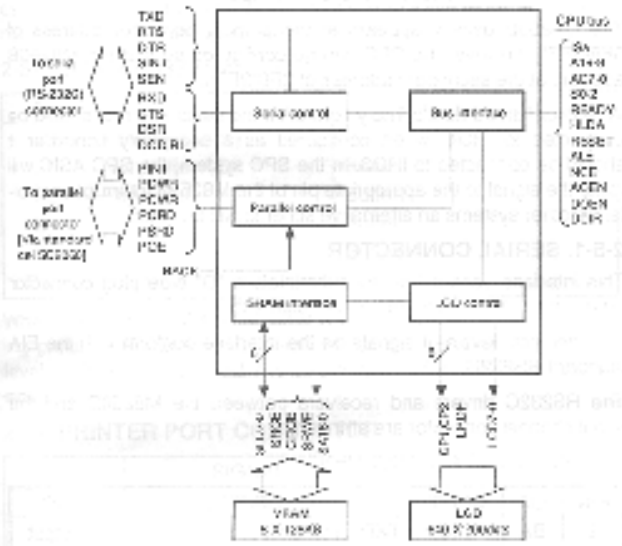


Fig. 2-1. DVC Block diagram

2-3. DVC I/O MAP

ADDRESS (hex)	DEVICE INPUT	DEVICE OUTPUT	NOTE
278	Printer data latch	Printer data latch	※1
279	**	Printer status	※1
27A	Printer control latch	Printer control latch	※1
27B-27F	**	**	
2F8-2FF	M82508 serial controller	M82508 serial controller	※2
378	Printer data latch	Printer data latch	※1
379	**	Printer status	※1
37A	Printer control latch	Printer control latch	※1
37B-37F	**	**	
3B0, 3B2, 3B4, 3B6	MDA 6845 address register	**	※3
3B1, 3B3, 3B5, 3B7	MDA 6845 data register	MDA 6845 data register	※3
3B8	MDA control register	**	※3
3B9	**	**	※3
3BA	MDA status	MDA status	※3
3BB	**	**	※3
3BC	Printer data latch	Printer data latch	※1
3BD	**	Printer status	※1
3BE	Printer control latch	Printer control latch	※1
3BF	**	**	
3D0, 3D2, 3D4, 3D6	CGA 6845 address register	**	※3
3D1, 3D3, 3D5, 3D7	CGA 6845 data register	CGA 6845 data register	※3
3D8	CGA mode control	**	※3
3D9	CGA colour select	**	※3
3DA	**	CGA status register	※3
3DB	Clear light pen latch	**	※3
3DC	Set light pen latch	**	※3
3DD	**	**	※3
3DE	ATT Register	ATT Register	※4
3DF	**	**	※3
3F8-3FF	M82508 serial controller	M82508 serial controller	※2
8400	SPC I/O <key register	**	

** Due to partial decoding of addresses, these addresses should not be used.
Addresses above 3FFh, if accessed, wrap and are mapped onto the range 000-3FFh. Address 8400h does not wrap as expected, this holds the access key to the SPC specific I/O.

※1 The parallel printer port may be configured to appear at its primary address of 378-37Fh, or its secondary address of 278-27Fh, or the MDA printer port address of 3BC-3BFh. The printer port may also be disabled.

※2 The M82503 serial port may be configured to appear at its primary address of 3F8-3FFh, or its secondary address of 2F8-2FFh. The M82508 serial port may also be disabled.

※3 The LCD controller may be configured to appear as an CGA/AT emulation at address 3D0-3DFh, or a MDA emulation at address 3B0-3BB. The LCD controller may also be disabled.

※4 The ATT register only appears if AT mode is selected.

2-4. DVC CONTROL I/O MAP

2-4-1. General

The DVC control registers are accessable only when unlocked by writing 44h to location 8400h. When a value other than 44h is written to 8400h, the registers are locked.

When the control registers are unlocked the normal I/O at address 000-3FFh does not wrap as expected.

ADDRESS (h)	REGISTER	COMMENT
8400	Key register	Write only
8402	ENABLE	I/O configure
8403	SRPS	SRAM page select
8404	LIND	LCD index
8405	LDTA	LCD data
8406	PMEN	Power Management
FFFF	TEST	For Manufacturing Test, write only

2-4-2. KEY REGISTER (8400h)

To unlock the SPC control I/O a value of 44h must be first written to this register, if any other value is written the SPC control I/O will be relocked.
NOTE. 44h is ASCII "D"

2-4-3. ENABLE

DVC configuration:-

(1) PARALLEL PRINTER PORT

D1	D0	FUNCTION
0	0	PPI is disabled (PP in low power mode)
0	1	PPI enabled at primary address of 378-37Fh
1	0	PPI enabled at secondary address of 278-27Fh
1	1	PPI enabled at MDA address of 3BC-3BFh

(2) M8250B SERIAL CONTROLLER

D3	D2	FUNCTION
0	0	M8250B is disabled (CLK off)
0	1	M8250B enabled at primary address of 3F8-3FFh
1	0	M8250B enabled at secondary address of 2F8-2FFh
1	1	M8250B is disabled (CLK off)

(3) VIDEO CONTROLLER MODE

D5	D4	FUNCTION
0	0	All video controllers are disabled (CLK off)
0	1	MDA enabled
1	0	CGA enabled
1	1	ATT enabled

D7 & D6 are not implemented and will be read back as '0'.

2-4-4. SRPS

Only used in 8088 MIN & 8088 MAX modes.

D6-0 are used for offset address in 2K pages (64 pages supported).

When DVC is used with 8088 min & 8088 max modes operation this register allows all 128K of memory supported by the DVC to be mapped into CPU address space (allowing character tables and RAM disc to be used).

D7 Disable wrapping.

D7 may be used to turn off wrapping usually associated with the MDA and CGA, when set (D7=1) 32K of DVC memory is directly accessible without paging, starting at the base address associated with the video mode selected (see 2-8. DISPLAY MEMORY MAP).

2-4-5. LIND section

Index address register for LCD configuration.

2-4-6. LDAT

LCD configuration data.

See section 2-7. LCD VIDEO CONTROLLER

2-4-7. PMEN

This register shadows a register in the SPC ASIC which controls power management.

Bits 7-4, and 2 of this register are not implemented in the DVC and will be read back as '0'.

D3 - LCD power:

When high LCD outputs and the DCC output are enabled.

D1 - Parallel Port buffer power:

when high Parallel Port outputs are enabled.

D0 - 1.9V supply:
When high Serial Port Buffers have power i.e.
When low Serial Port output should be tristate.

2-4-8. TEST

This register is used only for device test and is used to multiplex blocks of circuitry to the I/O pins of the device. It is therefore not available for software use. The bits of the register are assigned as follows:

D0 - '1' selects the M82508 block for test
D1 - '1' selects the line buffer RAM for test
D2 - '1' selects the D6845 block for test
D3 - '1' selects the tri-state leakage test
D4 - '1' selects the frame frequency test
D5 - '1' selects the parameter test

The register is reset to '0'. It is assumed that only one test mode will be selected at a time.

2-5. RS232C ASYNCHRONOUS SERIAL PORT

The asynchronous serial port is based on the M82508, single channel device.

The clock frequency input of the M82508 is 1.8432 MHz (0.1%). This clock is active when the M82508 is enabled. The 1.8432 MHz clock is derived from the CPU clock of 10.00 MHz.

In normal use the BAUD OUT OUTPUT is connected directly to the RCLK input.

An interrupt level is available for uses by the M82508. The M82508 INT output may be connected to, or disabled from, the interrupt controller by software.

When the M82508 OUT2 output is driven low then the INT output is connected to an interrupt controller IRQ input.

The M82508 usually appears at the primary controller address of 3F8-3FFh, however the SPC can be configured so that the M82508 appears at the secondary address of 2F8-2FFh.

When configured as a primary controller, the serial interrupt should be connected to IRQ4. When configured as a secondary controller it should be connected to IRQ3. In the SPC system, the SPC ASIC will route the signal to the appropriate pin of the M8259A interrupt controller. In other systems an alternative scheme will be used.

2-5-1. SERIAL CONNECTOR

This interface uses a 25-way subminiature "D" type plug connector emulating a DTE (Data Terminal Equipment).

The electrical levels of signals on the interface conform with the EIA standard RS232C.

The RS232D drivers and receivers between the M82508 and the serial channel connector are all inverting.

(1) CONNECTOR ARRANGEMENT

PIN	EIA	CCITT	DESCRIPTION	I/O
2	BA	103	TXD - Transmit serial Data	Output
3	BB	104	RXD - Receive serial Data	Input
4	CA	105	RTS - Request to send	Output
5	CB	106	CTS - Clear to send	Input
6	CC	107	DSR - Data set ready	Input
7		102	Common return (Ground)	
8	CF	109	DCD - Data Carrier Detect	Input
20	CD	108	DTR - Data Terminal Ready	Output
22	CE	125	RI - Ring Indicator	Input

2-5-2. CLOCK GENERATION

It is not possible to generate 1.8432 MHz from 10.00 MHz using a simple divider, however by dividing using a fixed sequence it is possible to generate 1.8432 MHz with reasonable accuracy (on average).

The divide sequence is:- 5, 6, 5, 5, 5, 6, ...

This gives an average frequency of 1.8421 MHz which is 0.06% slow, but within the 0.1% required.

2-6. PARALLEL PRINTER PORT

The printer port provides a centronics-compatible interface. The timing of signals to the printer is under software control.

The printer port will normally appear at the primary address of 378-37Fh, however it may be configured to appear at the secondary address of 278-27Fh or MDA address of 3BC-3BFh.

This port is implemented using latches and buffers external to the DVC ASIC. This is to save pins and to ensure correct buffering for the interface.

2-6-1. DATA LATCH (378h or 37Ch)

The data latch is 8 bit Output/Input.

The contents of the data latch are undefined following a power-up or system reset. Data is read back from a latch inside the DVC.

2-6-2. CONTROL LATCH (37Ah or 37Eh)

BIT	Output/Input
D7-6	No effect
D4	Enable interrupt on ACK
D3	Select printer
D2	Not reset printer
D1	Select auto feed
D0	Data strobe

All bits of the printer control latch are cleared by reset.

The timing requirements on centronics printers generally specify that the data must be present at least 1μS before the strobe is made active, and must remain valid for at least 1μS after the strobe. The duration of the strobe must be between 1uS and 500μS. The status can be inspected as soon as the strobe is inactive in order to determine when more data can be sent.

2-6-3. STATUS (379h or 37Dh)

Bit	Input	Connector input Buffer type
D7	Not printer busy	Inverter
D6	Not printer ACK	Buffer
D5	Paper out	Buffer
D4	Printer selected	Buffer
D3	Not printer error	Buffer
D2-0	Undefined	

When interrupt on ACK is enabled in the printer control latch, incoming printer Acknowledge condition will cause a system interrupt on level 7. Note interrupt level 7 is also available for use on the expansion bus.

2-6-4 PRINTER PORT CONNECTOR

2PIN	SIGNAL	TYPE
1	Not Data Strobe	Output/(Input)
2	Data 0	Output
3	Data 1	Output
4	Data 2	Output
5	Data 3	Output
6	Data 4	Output
7	Data 5	Output
8	Data 6	Output
9	Data 7	Output
10	Not printer ACK	Input
11	Printer busy	Input
12	Paper out	Input
13	Not printer select	Input
14	Not select auto feed	Output/(Input)
15	Not printer error	Input
16	Not printer reset	Output/(Input)
17	Select printer	Output/(Input)
18-25	Ground (0 volts)	

(Input) These signals are usually driven by open collector drivers, however in this application where power saving is vital they will be output only, should an external device drive one of these outputs it will be protected by a suitable series resistor (to be decided).

2-6-5. IMPLEMENTATION OF PARALLEL PORT HARDWARE

The parallel port hardware implementation uses external buffers and latches in order to reduce the external pin-count and to ensure the correct drive levels and strengths.

(1) Data Latch-should be implemented as an octal edge triggered latch, the strobe for the latch is pdw. The read-back path for this latch is from a register inside the DVC.

(2) Control Latch-should be implemented as an edge triggered latch, strobed by PCW. Bit 4 of this register is implemented inside the DVC, and the NACK signal from the interface should be connected to the DVC and this is used to drive the parallel port interrupt line. PCR is the read strobe for this port.

(3) Status Port-The read strobe (output enable for a buffer) for this port is PSR.

All the parallel port strobes are active low. Data bus connections are either direct to the CPU AD bus, or via a buffering scheme such as the one used for ISA (PC) bus mode.

2-7 LCD VIDEO CONTROLLER

This section should be read in conjunction with D6845 VIDEO CONTROLLER.

To allow the use of smaller LCDs than 640 x 200 or 640 x 400 various configuration registers have been provided, these configuration registers are only accessible when the SPC control I/O has been unlocked, via the register at 8403h.

2-7-1 STATUS CONTROL

Status lines are displayed at the end of active MDA, CGA or ATT display. The status display can be any length programmed. The length of the display is derived from the difference between the vertical total register and vertical displayed register (DSTV-DSV).

The status information starts at the location in SRAM indicated by SPC system configuration register DSST, the status information has same format as CGA graphics 640 x 200 (mode 6), but continuously in memory.

2-7-2 LCD CONTROL REGISTERS

The following registers are available when the SPC configuration I/O has been unlocked at address 8401 & 8405.

8404h is the index register (4 bit)

8405h is the Data register

INDEX	REGISTER	COMMENT
0	DTH	Horizontal display + border in characters.
1	DSH	Horizontal display size in characters.
2	MALT	Number of line per LCD DF signal alternation
3	TPVS	Top Panel Vertical Size
4	DSTV	Vertical display + Status in pixels.
5	DSV	Vertical display in pixels.
6	DSOL	LCD offset address.
7	DSOU	(in characters)
8	MCR0	Mode Control Register 0
9	MCR1	Mode Control Register 1
10	DSST	Display status start address/512.
11	DSCT	Character table start address/512.
12	DSGS1	Gray scale set GS1.
13	DSGS2	Gray scale set GS2.
14	DCC	Contrast voltage.

(1) DTH
This 8 bit register defines the horizontal display width in characters of the LCD and the number of character periods which the LCD controller waits before starting the next line.

(2) DSH
This 8 bit register defines the horizontal display width of the LCD in characters.

(3) MALT
This 8 bit register defines the number of line periods between an alternation of the phase of the LCD DF alternating signal. This can be used to enhance the sharpness of some LCD displays.

(4) TPVC
This 8 bit register defines the size of the top display. This is used in the situation where two LCD panels of unequal size are used to form the display.

(5) DSTV
This 8 bit register defines the vertical total in pixels of the LCD display, this is made of two parts, the display height in pixels and the status height in pixels.

(6) DSV
This 8 bit register defines the vertical display height in pixels.

(7) DSOU + DSOL
This 16 bit register defines the number of memory locations to the top left corner of the LCD, from the address defined in D6845 R12 & R13.

(8) EXAMPLES OF HOW THESE REGISTERS ARE USED
Single Display: 200 Line LCD. 4 Status lines to be displayed
DSTV=200
DSV=196
TPVC=X i.e. it is ignored
Double Display. 2 200 Line LCD Panels, 4 Status line to be displayed
DSTV=200
DSV=196
TPVC=200
Double Display: Top LCD 200 line, bottom LCD 100 lines, 10 status lines
DSTV=200
DSV=90
TPVC=200

(9) MCR0

Mode control register 0

BIT	NAME	COMMENT
D7	THN	If = 1 in 40*25 alpha, each PEL is 1 pixel wide not 2
D6	LLB	If = 1 blank last line if IBM standard character font
D5	PWD1	Defines the LCD interface data width as 1, 2,
D4	PWD0	4 or 8 bits
D3	INV	If = 1 all LCD data is inverted
D2	ULI	If = 0 underline is on scan 7, if = 1 scan 8
D1	CWD1	Defines horizontal size of character. 6, 7, 8 or
D0	CWD0	9 PEL, only applicable in alpha modes.

PEL = Picture Element, a PEL may be 1 or more pixels in size.
CWD1 & CWD0 when set to 9, the ninth PEL is always background colour.
LLB - Note the following.
BLANK DETECTION ALGORITHM
In order to save power, the DVC does not do any unecessary accesses to external SRAM in order to fetch data for the video display. In Alpha modes a line buffer is used to store character and attribute data. During the first scan of a character row this buffer is filled, during subsequent scans it is only necessary to fetch font data. However, if the character font information to be fetched is known to have no bits set - i.e. it is a space or the last row of most characters - then no font data is fetched either. The characters which will cause the DVC to fetch font information on the last row are:

05h - Box character
09h - Box character
5Fh - Underline
Any character with a character code > B0h

This feature can be switched off using bit 6 of MCR0. this allows the use of non standard character sets.
Note that the blank character (20h) will never be fetched from the font RAM, irrespective of the state of LLB.

(10) MCR1

Mode control register 1

BIT	NAME	COMMENT
D4	LKMDA	Lock MDA. Fixes character size to 8 rows in MDA mode
D3	DLC	If = 1 LCD screen is made using two LCD panels dimensions of which are defined using DSHL, DSHU, DSV.
D2	DUP	If = 1 all pixels are duplicated.
D1	SHF	If = 1 scans are quadrupled.
D0	SHT	If = 1 scans are duplicated.

SHT & SHF

D1	D0	Comment
0	0	Each scan is only displayed once.
0	1	Each scan is displayed twice
1	x	Each scan is displayed four times.

(11) DSST
Status Start address, this defines from which 512 byte boundary in SRAM the status information is to be found.
Status information has same format as CGA graphics mode 2. The display will be as per CGA graphics mode 2. i.e. it will not be affected by MCR1.
N.B. For status to work correctly where there are two LCD panels of unequal size being used, then either the top panel should be smaller than the lower one, or only eight bit characters should be used, with MCR1 set to 0h.

(12) DGCT
Start Character Table, this register defines from which 512 byte boundary in SRAM the character table starts.

(13) DSGS1
Each bit indicates if a PEL of GS1 is on (=1) or off (=0) during this frame.
D0 = 1 PEL of GS1 is on during frame 1.
D1 = 1 PEL of GS1 is on during frame 2.
etc...
D7 = 1 PEL of GS1 is on during frame 8.

(14) DSGS2
Each bit indicates if a PEL of GS2 is on (=1) or off (=0) during this frame.
D0 = 1 PEL of GS2 is on during frame 1.
D1 = 1 PEL of GS2 is on during frame 2.
etc...
D7 = 1 PEL of GS2 is on during frame 8.

(15) DCC
See section 2-10. CONTRAST CONTROLLER

2-7-3. ATT MODE

The LCD display used for ATT mode is made of two identical panels. The values used to define the display size are for any panel.

2-8. DISPLAY MEMORY MAP

The following table shows how the Display RAM for the various main display modes is mapped onto CPU memory address space when the Display Controller is enabled -

CPU Address	MDA Map	CGA Map	ATT Map
BFFFFh : B8000h		Repeat of CGA 16K block	ATT Modes 32K
B7FFFh : B4000h		CGA Modes 16K block	
B3FFFh : B1000h	7 repeats of MDA 4K block (28K)		
B0FFFh : B0000h	MDA Mode 4K		

The above mapping is only valid when the DVC ASIC is in either 8088 MIN or 8088 MAX modes, when in 8088 MAX + Memory Map mapping depends on how memory mapping registers have been configured.

2-8-1. TEXT DISPLAYS

Each character position displayed in text modes is represented by a pair of contiguous bytes in display RAM. The even addressed byte of each pair stores a character code which determines which of 256 different characters is to be displayed, while the odd byte stores a character attribute which determines how the character is to be displayed in terms of colour, reverse video, underlining, blinking etc.

(1) TEXT DISPLAY RAM MAPPING

The following tables show how the character codes and attribute bytes stored in RAM relate to the display for the various text modes.

Text Mode Memory Organization

Memory Address for CRTC start address = 0			Character No & Byte Type	Comment
MDA Text80	CGA Text80	CGA Text40		
B0000h B0001h	B8000h B8001h	B8000h B8001h	0 Code 0 Attr	1st character position (top LH corner)
B0002h B0003h	B8002h B8003h	B8002h B8003h	1 Code 1 Attr	2nd character position (1st row 2nd column)
:	:	:	:	
		B87CEh B87CFh	1999 Code 1999 Attr	Text40 last position (25th row 40th column)
		:	:	
B0F9Eh B0F9Fh	B8F9Eh B8F9Fh		3999 Code 3999 Attr	Text80 last position (25th row 80th column)

Text Mode Display Organization

The first displayed character in the top left corner of the screen (row 0, column 0) is that whose module 16K character code byte address ÷ 2 is programmed into the M6845 CRTC's 14 bit Start Address register; the above tables assume a start address of 0000h.

The memory space normally available for displaying MDA text is 4K bytes (2K characters).

The memory space available for displaying CGA text is 16K bytes (8K characters).

2-8-2. CGA GRAPHICS

In both CGA Graphic640 and Graphic320 modes the CRTC is programmed for 100 rows of characters of 2 scans each, and a character represents two bytes stored in RAM, one for the even scan and one for the odd scan. (Graphic160 mode, a very low resolution 160†100 dots in 16 colours, is not strictly graphics at all, but just a special application of Text80 mode with only two scans per row, which uses some half-block characters from the font to give two 'dots' per character. This mode will not be discussed further).

The bytes for the even scans 0, 2, 4 – – – – –, 196, 198 are stored in the first half of 16K RAM starting at B8000h, and those for the odd scans 1, 3, 5, – – – – – 197, 199 are stored in the second half starting at BA000h.

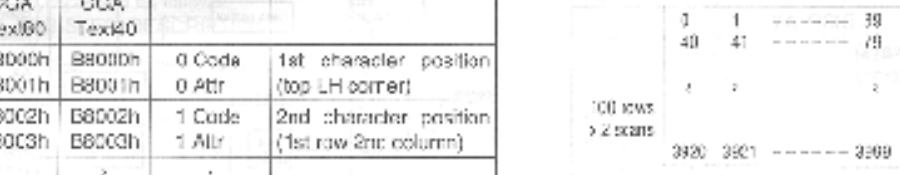
(1) GRAPHICS DISPLAY RAM MAPPING

The following tables show how the bytes stored in RAM relate to the display for the various graphics modes.

CGA Graphic320 & Graphic640 Memory Organization

RAM Addr for CRTC Start = 0	Char No	Scan No	Comment
		(Odd)	
B8000h	0	1	1st position (top LH corner)
B8001h	1	3	2nd position (1st row 2nd column)
:	:	:	
B9F3Fh	7999	199	Last position (100th row 80th column)
		(Even)	
BA000h	0	1	1st position 2nd scan
BA001h	1	1	2nd position 2nd scan
:	:	:	
BBF3Fh	7999	199	last position 2nd scan, bottom RH corner (ie 200th displayed scan)

CGA Graphics Display Organization



The first displayed character in the top left corner of the screen (row 0, column 0) is that whose module 16K even byte address ÷ 2 is programmed into the M6845 CRTC's 14 bit Start Address register; the above tables assume a start address of 0000h. It follows that a Graphic320 display may only be offset horizontally in 8 dot increments, and a Graphic640 display in 16 dot increments. Both modes may only be offset vertically in 2 scan increments.

The memory space available for displaying CGA graphics is 16K bytes (4K characters).

2-9. LCD COLOUR MAP

This section should be read in conjunction with MDA VIDEO CONTROLLER and CGA VIDEO CONTROLLER sections.

2-9-1. LCD GRAY SCALE

The LCD supports 4 gray levels these are: GS0 (OFF), GS1, GS2 & GS3 (ON). Grey levels are made by turning pixels on and off on an eight frame cycle.

GS0, is always off.
GS1, DSGS1 bits D0-7 define which frames in eight the PEL is on.
GS2, DSGS2 bits D0-7 define which frames in eight the PEL is on.
GS3, is always on.

DSGS1 & DSGS2 are LCD control registers.

2-9-2. MDA MAPPING

LEVEL	DISPLAY
GS0	Normal white on black, background Inverse black on white, foreground
GS1	Normal white on black, foreground Inverse black on white, background
GS3	Normal white on black highlighted, foreground Inverse black on white highlighted, background

2-9-3. CGA MAPPING

(1) ALPHA MODES

The two alpha modes 80 x 25 (high resolution) & 40 x 25 (low resolution) are mapped as follows:-

LEVEL	DISPLAY
GS0	Black background or foreground
GS1	Coloured background Coloured foreground if = background (except black)
GS2	Coloured foreground
GS3	Intensified foreground

(2) GRAPHICS MODES

① GRAPHICS MODE 1 (320 x 200)

Three palettes are mapped as follows:-

LEVEL	DISPLAY
GS0	Bit 1 = 0, Bit 0 = 0 Background
GS1	Bit 1 = 0, Bit 0 = 1. or Background if = colour.
GS2	Bit 1 = 1, Bit 0 = 0. or Background if = colour.
GS3	Bit 1 = 1, Bit 0 = 1. or Background if = colour.

② GRAPHICS MODE 2 (640 x 200)

This is a monochrome display the mapping is as follows:-

LEVEL	DISPLAY
GS0	Background (always) Foreground if = black
GS1	Not used
GS2	Not used
GS3	Foreground

2-9-4. ATT MODE

Mapping is the same as CGA, the additional ATT mode is same as CGA graphics mode 2.

2-10. CONTRAST CONTROLLER

2-10-1. INTRODUCTION

This 8bit register controls the duty cycle of the CDC output. The CDC output is used to control the contrast voltage of an LCD display (-VEE).

2-10-2. CONTRAST CONTROLLER I/O

SIGNAL	TYPE	DESCRIPTION
D6-0	Input	Data
NRST	Input	Reset
CCLK	Input	Clock 10MHz
CDC	Output	Variable mark space 0/128 to 128/128 at 500Hz.

(1) DATA (D7-0)

D7-0 are the data inputs D0 corresponds to bit 0 of the register.

(2) CLOCKS (CLK & CDC)

The CDC output is derived from the 10MHz system clock, this is first divided by 256, then by 128 to produce the CDC output. The duty cycle of the CDC output will depend on the value programmed in the the DCC register.

2-10-3. CONTRAST CONTROL REGISTER DCC

This eight bit register defines the contrast duty cycle.

If DCC = 00h then CDC will be low (continuous).
If 30h > DCC > 00h CDC duty cycle is dependent on DCC value.
If DCC > = 80h then CDC will be high (continuous).

3. SPC ASIC (TC146G68)

3-1. General

The SPC is ASIC having the following functions.

<CPU interface>

- Generation of various kinds of interruption
- CPU bus contro
- Expansion bus control

<Memory interface>

- Memory mapper
- Local memory control
- DMA controller

<Device controls>

- DVC control
- Keyboard control
- Sound control
- Power control

3-2. Block diagram

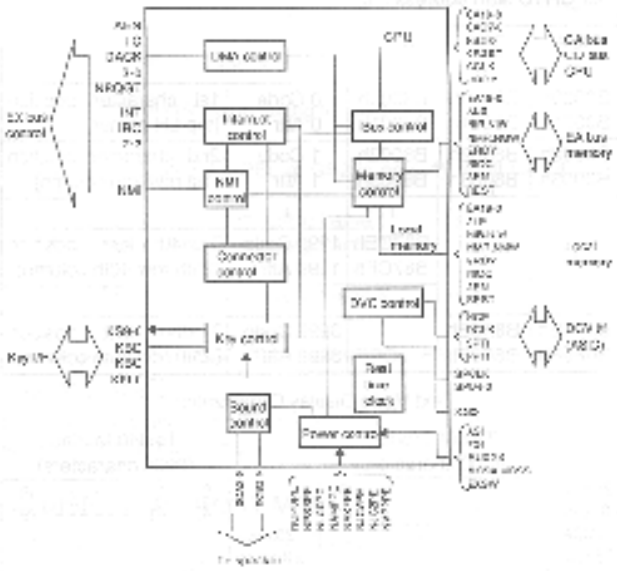


Fig 3-1. SPC BLOCK DIAGRAM

3-3. SPC I/O MAP

ADDRESS hex	DEVICE INPUT	DEVICE OUTPUT
000-00F	M8237A DMA controller	M8237A DMA controller
010-01F	**	**
020-021	M8259A interrupt controller	M8259A interrupt controller
022-03F	**	**
040-043	M8253 PIT controller	M8253 PIT controller
044-05F	**	**
060	**	M8255 port A
061	M8255 port B	M8255 port B
062	**	M8255 port C
063-07F	**	**
080	**	**
081	DMA page register 2	**
082	DMA page register 3	**
083	DMA page register 0 & 1	**
084-09F	**	**
0A0	NMI mask contro bit	**
8400	SPC I/O Key register	**

** Due to partial decoding of addresses, these addresses should not be used.
Addresses above 3FFh, if accessed, wrap and are mapped on to the range 000-3FFh. Address 8400h does not wrap as expected, this holds the access key to the SPC specific I/O.
Accesses to devices within the SPC or DVC ASICs do not appear on the expansion bus, however NMI mask register does.

3-3-1 MAPPING REGISTER I/O

The 64 page registers are accessed through three consecutive addresses in I/O space. An SPC configuration register selects the base I/O address to be used for page register access.

Page registers are accessed as follows:-
I/O ADDRESS, REGISTER, DESCRIPTION

BASE + 0	PRN5-0	Page register select
BASE + 1	PRN5-0	Page register select
BASE + 2	MA-8	Mapping address bit
BASE + 3	MA15-9	Mapping address msb

BASE+0 and base +1 are both mapped to the same register.
Usual addresses for Mapping registers are :-
208h, 218h, 228h, 238, etc..., 2E8 & 2F8.

Care must be taken when selecting an I/O address for the mapping registers that it does not conflict with other devices or uses reserved I/O locations.

3-4 SPC CONTROL I/O MAP

When the SPC control I/O is unlocked the normal I/O at address 000-3FFh does not wrap as expected within its address range.

I/O at these addresses can only be accessed if it has been unlocked. however address 8400h is always accessable.

3-4-1 SPC CONTROL I/O TABLE

ADDRESS (h)	REGISTER	COMMENT
8400	Key register	01h read back when unlocked
8401	LIMIO	Memory map I/O base
8402	ENABLE	I/O configure
8403	SRPS	SRAM page select 1
8404	LIND	LCD index register 1
8405	LDAT	LCD data 1
8406	PCNTR	Power control register
8407	CCNTR	Clock control register
8408	CPOS	CPU clock speed

ADDRESS (h)	REGISTER	COMMENT
8409	ROMP	JEIDA programming control
840A	PASR	M8255 status latch
840B	PASR	
840C	NMI08	SPC NMI vectors
840D	NMI09	
840E	NMI0A	
840F	NMI0B	
8410	SISR	SPC interrupt source register
8411	SISE	SPC interrupt enable
8412	PSIR	Power supply int. register
8413	PSIE	Power supply int. enable
8414	PSIS	Power supply status
8415	ISIR	Internal service int. register
8416	ISIE	Internal service int. enable
8417	MIR	Memory int. register
8418	MIR	Memory int. enable
8419	MIS	Memory status
841A	RSTR	CPU reset source register
841B	KSTR	LCD Status Register
841C-84 1F	**	
8420	ATR0	Address map
8421	ATR1	
8422	ATR2	
8423	**	
8424	MAV0	Memory access violation
8425	MAV1	
8426	MAV2	
8427	**	
8428	ACR lsb	Activity register
8429	ACR	
842A	ACR msb	
842B	ACM	Activity mask register
842C	SWG1	Sound channel 0
842D	SWG0	
842E	SWG1	Sound channel 1
842F	SWG1	
8430	SCR-ISCR	Keyboard
8431	ARR	Keyboard auto repeat
8432	PDR lsb	Keyboard power down
8433	PDR msb	
8434	WSR0	Keyboard warm start
8435	WSR1	
8436	WSR2	
8437	SKWR	Single key wake-up
8438-F	**	
8440	TCR lsb	DTC Tick Count Register
8441	TCR	
8442	TCR	
8443	TCR msb	
8444	TKI lsb	DTC Tick interrupt register
8445	TKI	
8446	TKI	
8447	TKI msb	
8448	TMI lsb	DTC Timer interrupt register
8449	TMI	
844A	TMI	
844B	TMI msb	
844C-F	**	
8450	RTR lsb	RTC counter register
8451	RTR	

ADDRESS (h)	REGISTER	COMMENT
8452	RTR	
8453	RTR	
8454	RTR msb	
8455-57	**	
8458	RTI lsb	RTC interrupt register
8459	RTI	
845A	RT	
845B	RT	
845C	RT msb	
845D	TR	DTC timer control register
845E-F	**	

1 These registers are not in the SPC ASIC.

3-4-2 KEY REGISTER (8400h)

To unlock the SPC control I/O a value of 44h must be written to this register, if any other value is written the SPC control I/O will be locked.

If the SPC control I/O is locked a value of 00 will be read from this register.
If the SPC control I/O is unlocked a value of 01 will be read from this register.

3-4-3 LIMIO (8401h)

This register defines the BASE address of the memory mapping registers (LIM) in I/O space.

D7-0 correspond to A9-A2 of I/O address.

3-4-4 ENABLE (8402h)

(1) PARALLEL PRINTER PORT

D1	D0	FUNCTION
0	0	PPI is disabled
0	1	PPI enabled at primary address of 378-37Fh
1	0	PPI enabled at secondry address of 278-27Fh
1	1	PPI enabled at MDA address of 3BC-3BFh

(2) M82500 SERIAL CONTROLLER

D3	D2	FUNCTION
0	0	M8250B is disabled
0	1	M8250B enabled at primary address of 3F8-3FFh
1	0	M8250B enabled at primary address of 2F8-2FFh
1	1	M8250B is disabled

(3) VIDEO CONTROLLER MODE

D5	D4	FUNCTION
0	0	All video controlers are disabled
0	1	MDA enabled
1	0	CGA enabled
1	1	ATT enabled

Bits D6 and D7 are undefined, they are read back as 0.

3-4-5 SRPS (8403h)

Only used in 8088 MIN & 8088 MAX modes

Only D6-0 are used for offset address.

When the DVC is used with 8088 min & 8088 max modes operation this register allows all 128K of memory supported by the DVC to be mapped into CPU address space.

3-4-6 LIND (8404h)

Address register for LCD configuration.

See DVC ASIC specification section LCD VIDEO CONTROLLER.

3-4-7 LDAT (8405h)

LCD configuration data.

See DVC ASIC specification section LCD VIDEO CONTROLLER.

3-4-8 PASR REGISTERS (840Ah, 840Bh)

These two registers replace switches usually found on a PC mainboard, see M8255 section.

All other registers are defined in their relevant sections.

3-5. SPC INTERRUPTS

All interrupts in the SPC are listed below:

INT	TYPE	SOURCE	CLEARED
IR00	INT	PIT OUT0	M8259A
IR01	INT	Keyboard	M8259A
IR02	INT	Expansion bus	M8259A
IR03	INT	Expansion bus	M8259A
IR04	INT	Exp bus/Serial control	M8259A
IR05	INT	Expansion bus	M8259A
IR06	INT	Expansion bus	M8259A
IR07	INT	Exp bus/Parallel port	M8259A
IOCHK	NMI	I/O check on exp bus	Write M8255 PB5
KINT	NMI	Matrix keyboard	Read SCR
EXPI	NMI	Expansion unit switch	Read MIR
AABL1	NMI	AA battery level	Read PSIR
AABL0	NMI	AA battery level	Read PSIR
LIBL	NMI	Lithium cell level	Read PSIR
EXBL1	NMI	Expansion battery level	Read PSIR
EXBL0	NMI	Expansion battery level	Read PSIR
MABL	NMI	Memory card A batt level	Read PSIR
MBBL	NMI	Memory card B batt level	Read PSIR
ACPWR	NMI	AC Power level	Read PSIR
RTCINT	NMI	Real Time Clock	Read RTI
TICI	NMI	DTC tick timer	Read TKI
TIMI	NMI	DTC timer	Read TMI
SPCA	NMI	Activity detector	Read ACM
PATR	NMI	Address trap	Read ATR2
KBPD	NMI	Keyboard power down req	Read SCD
MCWPA	NMI	Memory card A write protect	Read MTP
MCWPB	NMI	Memory card B write protect	Read MTP
MCDA	NMI	Memory card A detect	Read MTP
MCDB	NMI	Memory card B detect	Read MTP
MAV	NMI	Memory access violation	Read MAV2
WINT	NMI	Matrix Keyboard Wake-Up	Read SISR
MCSA	NMI	Memory card A switch	Read MIR
MCSB	NMI	Memory card B switch	Read MIR
EXSW	NMI	Expansion Unit switch	Read MIR

3-6. M8259A INTERRUPT CONTROLLER

3-6-1 GENERAL DISCUSSION

Addressed at 020-03Fh.
Eight levels of hardware interrupt are supported by the M8259A interrupt controller.
The M8259A interrupt controller has A0 connected conventionally so that command codes appear in the expected order as in the M8259A specification. The M8259A is at address 020-021h.
In normal use SP/EN input is tied high indicating that the device is hardware un-buffered and designated as a master.

3-6-2 INTERRUPT LEVEL

The interrupt levels are assigned as follows:-

Level 0	M8253 PT OUT0
Level 1	Keyboard receive logic
Level 2	Available on expansion bus.
Level 3	Available on expansion bus (serial controller when enabled at secondary address)
Level 4	Available on expansion bus (serial controller when enabled at primary address)
Level 5	Available on expansion bus.
Level 6	Available on expansion bus.
Level 7	Available on expansion bus. (Parallel Printer Port when enabled)

3-6-3 M8259A INITIALISTATION

Following a system reset, system initialisation software should set the M8259A as follows:

8086 system
Single (not cascade)
Normally fully nested
Edge triggered
Buffered mode
Normal EOI
Fixed priority-level 0 highest, level 7 lowest.

3-7 NMI control

3-7-1 GENERAL DISCUSSION

There are two sources of NMI, those normally associated with PC systems and those generated by SPC specific features (ie SPC matrix keyboard KINT).

3-7-2 SYSTEM NMI

INTERRUPT SOURCE
NMI I/O Check from expansion bus

Note: No system memory is parity checked, nor is there a co-processor fitted (8087).
The expansion bus I/O Check input is enabled or disabled via M8255 PB5 (port B bit 5).
The IOCHK NMI (from the expansion bus) can be masked under software control (0A0h bit D7, write only).

3-7-3 SYSTEM NMI MASK

Addressed at 0A0h

D7	Output use
D7	Enable System NMI
D6-0	No effect

Following a reset, NMI is disabled.
CPU accesses to this register will also appear on the expansion bus.

3-7-4 SPC SPECIFIC NMI

The SPC has a set of special interrupt sources, these are from SPC specific blocks, such as power management, matrix keyboard etc.
When an SPC specific interrupt is acknowledged the NMI vector read by the CPU from memory addresses 00008-0000Bh is intercepted, and data held in system configuration registers NMI06-NMI0E is substituted.
If the NMI is non SPC specific (I/O check) the NMI vector is read from memory 00008-0000Bh as expected.
SPC specific interrupts may be read back from SPC status register SIGR as follows:-

INTERRUPT	SOURCE	REGISTER
		SISR D7
		SISR D6
WINT	Matrix keyboard	SISR D5
KINT	Matrix keyboard	SISR D4
PSINT	Power status	SISR D3
ISINT	Internal service	SISR D2
MCINT	JEIDA memory cards	SISR D1
MAVI	Memory access violation	SISR D0

This register is read only, reading the register will clear bits D7, 4 & 5.
All interrupts can be enabled/disabled by setting/clearing the corresponding bits if SISE register.
Bit D6, D7 are always read back as 0.

3-7-5 PSINT

The source of the PSINT can be read from the PSIR register as follows:

Interrupt	source	register
AABL1	AA batteries low	PSIR D7
AABL0	AA batteries flat	PSIR D6
LIBL	Lithium battery flat	PSIR D5
EXBL1	Expansion batteries low	PSIR D4
EXBL0	Expansion batteries flat	PSIR D3
MABL	JEIDA card A batteries low	PSIR D2
MBBL	JEIDA card B batteries low	PSIR D1
ACPWR	External power low	PSIR D0

This register is read only, reading the register will clear it.
All interrupts can be enabled/disabled by setting/clearing the corresponding bit in PSIE.
The status of the power sources can be read at any time from PSIS.
PSIS is updated once per millisecond.

3-8. MEMORY MAP

Memory space (1 M byte) is divided into 64 16K page each page having an associated mapping register, all mapping registers are programmable.
Both CPU and DMA cycles will also be protected during DMA cycles.

3-8-1 MEMORY MAP REGISTERS

Table of memory mapping registers and their associated address range.

No	Address lo		COMMENTS
0	00000	03FFF	
1	04000	07FFF	
2	08000	0BFFF	
3	0C000	0FFFF	
4	10000	13FFF	
5	14000	17FFF	
6	18000	1BFFF	
7	1C000	1FFFF	
8	20000	23FFF	
9	24000	27FFF	
10	28000	2BFFF	
11	2C000	2FFFF	
12	30000	33FFF	
13	34000	37FFF	
14	38000	3BFFF	
15	3C000	3FFFF	256K boundary
16	40000	43FFF	
17	44000	47FFF	
18	48000	4BFFF	
19	4C000	4FFFF	
20	50000	53FFF	
21	54000	57FFF	

No	Address In		COMMENTS
22	58000	5BFFF	
23	5C000	5FFFF	
24	60000	63FFF	
25	64000	67FFF	
26	68000	6BFFF	
27	6C000	6FFFF	
28	70000	73FFF	
29	74000	77FFF	
30	78000	7BFFF	
31	7C000	7FFFF	512K boundary
32	80000	83FFF	
33	84000	87FFF	
34	88000	8BFFF	
35	8C000	8FFFF	
36	90000	93FFF	
37	94000	97FFF	
38	98000	9BFFF	
39	9C000	9FFFF	640K boundary
40	A0000	A3FFF	
41	A4000	A7FFF	
42	A8000	ABFFF	
43	AC000	AFFFF	
44	B0000	B3FFF	Used by MDA
45	B4000	B7FFF	Used by MDA
46	B8000	BBFFF	Used by MDA
47	BC000	BFFFF	Used by MDA
48	C0000	C3FFF	
49	C4000	C7FFF	
50	C8000	CBFFF	
51	CC000	CFFFF	
52	D0000	D3FFF	
53	D4000	D7FFF	
54	D8000	DBFFF	
55	DC000	DFFFF	
56	E0000	E3FFF	
57	E4000	E7FFF	
58	E8000	EBFFF	
59	EC000	EFFFF	
60	F0000	F3FFF	60-63 Used by BIOS
61	F4000	F7FFF	
62	F8000	FBFFF	
63	FC000	FFFFF	

Following a system reset the memory mapping registers will be disabled and all memory accesses will be mapped to device 0 (OTPROM0) page 4095. While disabled the mapping registers can be accessed by the CPU and software should set up all registers even if some are not used. When the msb of register 63 has been written the mapping registers will be enabled.

3-8-2 MAPPING REGISTER FORMAT

(1) MAPPING REGISTER I/O

The 64 page registers are accessed through three consecutive addresses in I/O space. An SPC configuration register selects the base I/O address to be used for page register access.

Page registers are accessed as follows:

I/O ADDRESS	REGISTER	DESCRIPTION
BASE + 0	PRN5-0	Page register select
BASE + 1	PRN5-0	Page register select
BASE + 2	M7-0	Page register data lsb
BASE + 3	M15-8	Page register data msb

BASE+0 and base+1 are both mapped to the same register.
After power-up all page registers are undefined.

(2) MAPPING REGISTER FORMAT

Each mapping register is 16 bits wide (M15-0), the bits are allocated as follows:

BIT FUNCTION
MA15-12 Device select
MA11-0 Address map and Read only Enable bits

① DEVICE SELECT

MA15-12	DEVICE	COMMENT
0	OTPROM0	
1	OTPROM1	
2	ROM0	
3	ROM1	
4	PSRAM0	
5	PSRAM1	
6	PSRAM2	Optional (may not be fitted)
7	PSRAM3	Optional (may not be fitted)
8	JEIDA A R/W	Read/Write
9	JEIDA A R	Read only
A	JEIDA B R/W	Read/Write
B	JEIDA B R	Read only
C	SRAM R/W	Read/Write
D	SRAM R	Read only
E	Expansion Bus	
F		No memory device selected

② PAGE SELECT
Read only devices (OTPROM0, OTPROM1, ROM0 & ROM1) and JEIDA cards
Up to 4096 page (12 bit MA11-0) of 16K byte can be selected (64M byte).
Devices with less than 4096 page will wrap.
The OTPROMs and ROMs are externally limited to 1M byte

③ PSRAM
Up to 256 pages (MA7-0) of 16K byte can be selected (4096K byte), this is externally limited to 1M byte.
Each of the 16K page is further divided into 4K segments, each 4K segment can be made either Read/Write (bit = 0) or Read Only (bit = 1), 4 bits usually used for paging (MA11-8) are allocated for this function.

BIT	BIT=0	BIT=1
MA8	4K segment 0 is R/W	4K segment 0 is Read only
MA9	4K segment 1 is R/W	4K segment 1 is Read only
MA10	4K segment 2 is R/W	4K segment 2 is Read only
MA11	4K segment 3 is R/W	4K segment 3 is Read only

If a PSRAM segment set Read only is written, a memory access violation interrupt is generated (NMI), and the write will fail.

④ SRAM
Up to 16 page (MA3-0) of 16K byte can be selected (256K BYTE).
For device select C, each of the 16K pages is divided into 2K segments, each 2K segment being made either Read/Write (bit = 0) or Read Only (bit = 1), 8 bits usually used for paging (MA11-MA4) are allocated for this function.

BIT	BIT=0	BIT=1
MA4	2K segment 0 is R/W	2K segment 0 is Read only
MA5	2K segment 1 is R/W	2K segment 1 is Read only
MA6	2K segment 2 is R/W	2K segment 2 is Read only
MA7	2K segment 3 is R/W	2K segment 3 is Read only
MA8	2K segment 4 is R/W	2K segment 4 is Read only
MA9	2K segment 5 is R/W	2K segment 5 is Read only
MA10	2K segment 6 is R/W	2K segment 6 is Read only
MA11	2K segment 7 is R/W	2K segment 7 is Read only

If SRAM device select D then whole 16K page is Read only irrespective of the state of MA11-MA4
If a SRAM page or segment which is set Read only is written, a memory access violation interrupt is generated (NMI), and the write will fail.

3-9. DIP KEYBOARD INTERFACE (DKI)

3-9-1 GENERAL DISCUSSION

The keyboard interface will produce a scan-code based on an 11*11 key switch matrix, allowing for a maximum of 121 keys. The interface will produces a scan-code between 0 and 78h (0-120). A flag indicating whether the scan-code was generated on a press or a release will be provided.

A key action will generate a keyboard interrupt (KINT). The processor will read the scan-code Register (SCR) to get the scan-code for that key action. The top bit will be set to indicate a key release. Only one interrupt for each press and each release will be generated. It is important that if an interrupt is sent to the processor, the scan-code of the key that generated that interrupt is read by the processor. Once a key press action has been read by the processor, and if no changes occur within a number of scans (dictated by the auto-repeat register (ARR)) then interrupts will be generated repeatedly each scan.

The keyboard controller will scan the 11*11 matrix, junction by junction. A counter will follow the scan and will thus be holding the current scan-code. This scan-code will be loaded into the SCR when that key state changes. The current state of the keyboard could be stored in a 121 bit shift register. Each bit would represent one key on the keyboard. Each register bit would store the value of the last key used (press or release). When the register and keyboard have different values, a toggle has occurred and a key action is detected.

A set of three registers (Warm Start Registers-WSR) will hold a set of scan-codes. When each of the three scan-codes are pressed on any one scan, a warm start will be generated. Warm start may be disabled by setting the WSRs to a value greater than 121.

The single key wake-up register (SKWR) will hold a scan-code in the 7 lsbs. When this scan code is found a wake-up interrupt (WINT) is generated. Setting this register to a value greater than 121 will disable the single key wake-up. The msb of this register is used to enable the cancel keyboard.

The keyboard interface contains a register called the scan-code Register (SCR). This will allow scan-codes to appear on in a PC.

Since the facility to power-down when no computer action is taking place is required, a scan counter is provided. This will count matrix scans until the count reaches the value stored in power-down Register (PDR). At this point an interrupt will occur. If the PDR is cleared then no power-down interrupt will be generated. When the PDR interrupt (PDI) is cleared, the counter will be reset. The PDR interrupt will be cleared by a read from the scan-code register or by a keyboard interrupt (KINT) occurring.

When the low Power Signal (LP) is low, all unnecessary counts will be terminated.

3-9-2 KEYBOARD CONTROLLER I/Os

SIGNAL	TYPE	DESCRIPTION
D7-0	Input	Data in
OD7-0	Output	Data out
A2-0	Input	Address
NRD	Input	Read strobe
NWR	Input	Write strobe
RST	Input	Reset
WRST	Output	Keyboard reset
KI10-0	Input	Scan input
OKI10-0	Input	Sense Input
KO10-0	Output	Scan output
PDI	Output	Power down interrupt
KINT	Output	Key scan interrupts
WINT	Output	Wake-up interrupt
LP	Input	Low power mode
WAKE	Input	Not used
NTST	Input	Test mode, only used during factory test

(1) Data bus (D7-0 & OD7-0)
These are the data bus connections. D0, OD0 will correspond to bit 0 of any registers.

(2) Address inputs (A2-0)
These inputs are used to decode which registers are selected within a KRD and KWR cycle. The register decoded is as follows:

A2	A1	A0	Register	TYPE
0	0	0	SCR	R
0	0	0	ISCR	W
0	0	1	ARR	R/W
0	1	0	PDR lsb	R/W
0	1	1	PDR msb	R/W
1	0	0	WSR0	R/W
1	0	1	WSR1	R/W
1	1	0	WSR2	R/W
1	1	1	SKWR	R/W

R = Read only, W = Write only, R/W = Read/Write.
A0 is the least significant address bit.

(3) Register control lines (NRD & NWR)
When NRD is low the contents of the register addressed by A0-A2 is placed on to the data bus. The rising edge of NWR will cause the value on the data bus to be latched in to the register decoded by A0-A2.

(4) Reset line (NRST)
When NRST is Low, all keyboard registers will be cleared.

(5) WARM START (WRST)
When all the warm start scan-codes have been found on a single scan, WRST line will pulse high for one KCLK cycle. This will cause a CPU reset and will set the KRST bit in the reset source register (RSTR).

(6) Scan lines (KI10-0, OKI10-0 & KO10-0)
KO0-KO10 are the keyboard scan outputs. KI0-KI10 are the keyboard scan inputs. OKI0-OKI10 are KO0-KO10 fed back as input to the ghost key detection circuit.
At any time, one only of KO0-KO10 will be driven high. (The others will be high impedance, but are pulled down to allow Ghost Key Detection to operate)
KI0-KI10 are pulled down. Each clock cycle of KCLK will cause the examination of each of KI0-KI10 in turn. If any of KI0-KI10 are high then that KI signal combined with the high KO signal will identify a pressed key. When each of KI0-KI10 has been examined, the high KO signal is changed and the KI scan is repeated. In this way the whole key matrix will be examined, one key at a time.

(7) Interrupt signals (PDI, KINT & WINT)
PDI will go high to indicate that the power-down count has been reached. This line is cleared by reading the scan-code register or by a keyboard interrupt (KINT) occurring.
KINT will go high to indicate that a key scan-code is waiting to be read by the processor. This line is cleared by reading the scan-code from the scan-code register.
WINT will go high for one KCLK period to indicate that the single key wake-up scan-code has been detected.

(8) Additional signals (LP, WAKE & NTST)
LP is high normally. If LP is low the keyboard circuit enters a low power mode. The ARR and PDR will stop counting to save power.
The WAKE input is unused and will be pulled high.
NTST is a test input used for testing DKI during device test.

3-9-3 KEYBOARD POWER-DOWN REGISTER PDR

This read/write 16 bit register is compared with the contents of a 16 bit counter. This counter is cleared on a key action or on writing to the PDR, and incremented each complete scan of the key board matrix if the PDR is non-zero. When the register and the counter match, a keyboard power down interrupt is generated.

3-9-4 KEYBOARD SCAN-CODE REGISTER SCR (Read only)

Reading this read-only register after a keyboard interrupt will return a valid 8 bit scan-code. This will be held in bits 0-6, giving a scan-code between 0 and 127 (only 0-120 are valid). Bit 7 will be cleared to 0 if the interrupt was for a key press and set to 1 for a key release. Reading this register will clear the keyboard and power-down interrupts. The key matrix is mapped onto the scan-code according to the following scheme:

Scan-code Matrix Position

HEX	DEC	SCAN	SENSE
00h	0	KO0	KI0
01h	1	KO0	KI1
.	.	.	
0Ah	10	KO0	KT10
0Bh	11	KO1	KI0
0Ch	12	KO1	KI1
.	.	.	
78h	120	KC10	KI10

3-9-5 PC KEYBOARD REGISTER ISCR (Write only)

This 8-bit register is write only, however it may read vi the M8255 port A (when selected). It is to be used for storing IBM format scan-codes for use with RC1.

The state of M8255 PB7 & PB6 (port B bits 7 & 6) should be checked to make sure it safe to write this register (i. e. keyboard has not been disabled by software), and IRQ1 in case the last keycode has not yet been read.

3-9-6 WARM START TRAP REGISTERS WSR0-WSR2

These are read/writeable. Each register is used to store an 8 bit scan-code. If all three of these specially selected scan-codes are found on any single complete matrix scan a warm start reset will be generated.

3-9-7 SINGLE KEY WAKE-UP REGISTER SKWR

This read/write register is used to store a 7-bit scan-code (bits 0-6). When this scan-code is found a single key wake-up interrupt is generated. Bit 7 is low to enable the on board matrix keyboard and is high to enable the external serial keyboard.

3-9-8 AUTO-REPEAT REGISTER ARR

This 8 bit read/write register holds the number of scans required before auto-repeat occurs. If no key strokes have occurred for this many scans and at least one key is pressed, then a periodic interrupt will be generated. This will cause the scan-code for the pressed key to be issued to the processor every scan.

3-9-9 GHOST KEY DETECTION

Since three keys or more pressed together may cause ghost keys to occur, a simple method of preventing this is required.

When the DKI detects a ghost key, it inhibits all further interrupts via KINT and preserves the state of key board matrix. After one complete scan of the keyboard matrix without a ghost key being detected, the DKI will start to generate interrupts again and will send key codes corresponding to the differences between the previous and the new state of the key matrix.