CHAPTER 5. LCD (LM64N671)

1. MAIN LCD (LM64074F)

1-1. Structure

Structure: The 640 x 200 full dot liquid display graphic display unit consists of an LCD panel, electronic component printed circuit board, and the film carrier LSI that electrically connected.

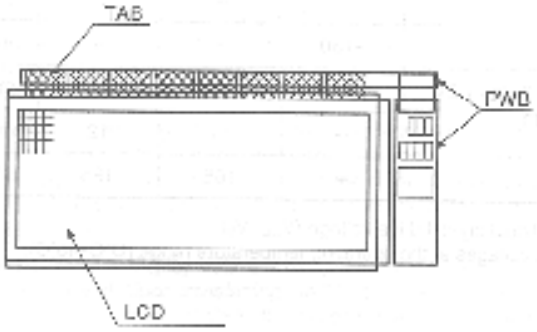
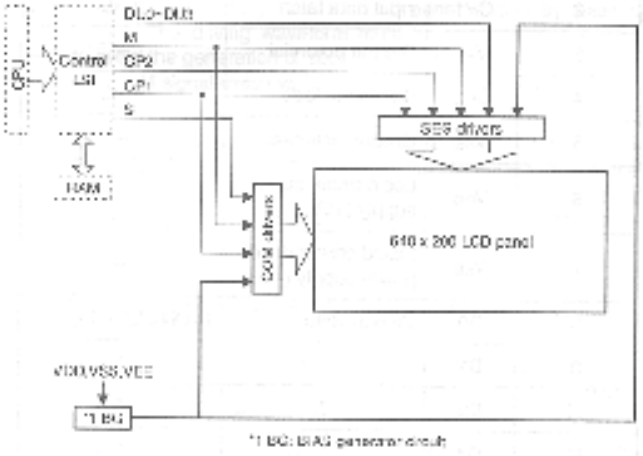


Fig. 5-1

1-2. BLOCK DIAGRAM



*1 BG: BIAS generator circuit

Fig. 5-2

1-3. Specification

Tbl. 5-1

Item	Characteristics	Unit
×1 Physical dimensions	206.5(W) x 85.5(H) x 4.5MAX(D)	mm
Effective display area	177.4(W) x 70.4(H)	mm
Display format	640(W) x 200(H) full dot	–
Dot size	0.24 x 0.30	mm
Dot space	0.03	mm
×3 Dot color	Black ×3	
×2 Background color	White ×3	–
Weight	About 68	g

×1: The physical dimensions of the unit excludes the LCD sealed portion.
×2: The color of the LCD panel may vary according to the environmental temperature due to the characteristic of the LCD panel.
×3: Data "H" → ON=black
Data "L" → OFF=white

1-4. Absolute maximum rating

(1) Absolute electrical maximum rating

Tbl. 5-2

Item	Symbol	Minimum	Maximum	Unit	Note
For logic circuit	$V_{DD} - V_{SS}$	0	6.0	V	Ta = 25°C
For liquid crystal drive circuit	$V_{DD} - V_{EE}$	0	28.0	V	Ta = 25°C
Input voltage	V_{IN}	0	V_{DD}	V	Ta = 25°C

(2) Environmental requirements

Tbl. 5-3

Item	Storage		Operating		Note
	Minimum	Maximum	Minimum	Maximum	
Temperature	–25°C	+80°C	0°C	+45°C	
Humidity	NOTE(1)		NOTE(1)		Free of moisture condensation

NOTE(*1): Ta ≦ 40°C . . . 95%RH, max.
Ta > 40°C . . . Absolute humidity must be 85%RH with Ta=40°C.

1-5. Electrical characteristics

(1) Electrical specification

Tbl. 5-4

Ta = 25°C, V_{DD} = 5V ± 5%

Item	Symbol	Condition	Minimum	Typical	Maximum	Note
For logic circuit supply voltage	V_{DD} – V_{SS}		4.75	5.0	5.25	V
For liquid crystal drive circuit supply voltage	V_{EE} – V_{SS}	(※1)	–6.5	–9.0	–12.3	V
Input voltage	V_{IN}	High level	0.8V_{DD}	–	V_{DD}	V
		Low level	0	–	0.2V_{DD}	V
Input leak current	I_{IL}	High level	–	–	150	μA
		Low level	–150	–	–	μA
For logic circuit supply current	I_{DD}	V_{DD}=5V, V_{DD}–V_{EE}=F=75Hz 21.2V High frequency pattern	–	13	15	mA
For liquid crystal circuit supply current	I_{EE}		–	11	12	mA
Power consumption	Pd		–	165	185	mW

(※1): The view angle (θ) of a maximum contrast may be obtained by changing the liquid crystal drive voltage (V_{DD}–V_0).
Maximum and minimum limits of the rating show the maximum and minimum voltages at the operating temperature range (0°C–45°C).
*Typical voltage is normal voltage at 25°C.

(2) Input capacity

Tbl. 5-5

Signal name	Input capacity
S	20pF TYP
CP1	200pF TYP
CP2	200pF TYP
D0–D3	200pF TYP

Line Sync
Line Clock
Pixel Clock
Frame Toggle

(3) Interfacing signals

[1] Connector

Pin No.※	Symbol	Function	Active signal level
1	S	Scan start	"H"
2	CP1	Input data latch	H→–
3	V_{SS}	Ground potential	–
4	CP2	Data input lock	H→I
5	V_{SS}	Ground potential	–
6	V_{DD}	Logic circuit power supply (+5V)	–
7	V_{EE}	Liquid crystal drive power supply (–)	–
8	D0	Display data	H(ON), L(OFF)
9	D1	"	"
10	D2	"	"
11	D3	"	"
12	M		

Tbl. 5-6

1-6. Driving method

1) Circuit configuration

Fig.6-2 shows the block diagram of the circuit configuration.

2) Display configuration

To obtain high contrast display by decreasing the duty, the area of 640 x 200 dots display is driven by 1/200 duty.

3) Input data and control signals

The LCD drive is 80-bit LSI that consists of shift register, latch circuit and LCD drive circuit.

A 4-bit parallel data is supplied to one line (640 dots) of both display sectors at a time, starting from the upper left corner of the display, via the shift register with the clock pulse CP2.

Upon receiving one line input data (640 dots), 640 signals are latched as parallel data at a high to low transition of the latch signal CP1 to supply dot drive signals corresponding to 640 electrodes of the LCD panel.

Since the scan start signal S sent to the scan signal drive circuit has been transferred to the first line of the scan electrode, the contents of the data signals are displayed on the first line of the display screen by a combination of the LCD scan electrode and the voltage added to signal electrode.

While the first line display data are being displayed, the second line data are received. Upon transferring the 640 dots data and latched at a high to low transition of CP1, the second line data are now displayed.

When data transfer is repeated down to the 200th line in this manner using the multiplex mode from the upper to lower lines, a single cycle of a full data display (1 frame) is completed, then again starts to accept the data from the first line. The scan start signal S is a horizontal electrode drive signals.

If a DC voltage was added to the LCD panel, a chemical reaction takes place in the liquid crystal of the LCD panel which may result in LCD fatigue. The driving waveform must be reversed in a certain cycle to avoid the generation of such a DC voltage. This is performed by the sync M signal circuit which converts the driving waveform into AC signal M.

On account of the characteristics of the CMOS driver LSI, the power consumption of the unit increases proportionate to the increase of the CP2 clock frequency. Therefore, to decrease the CP2 clock data transfer speed, the driver LSI incorporates the system to 4 bits transfer parallel data through 4 shift registers. Use of this LSI abates the power consumption of the unit.

For this circuit configuration, a 4-bit display data are supplied from data input lines of D0-3.

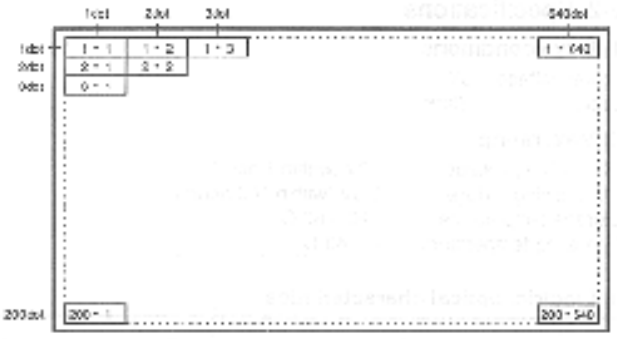
Aside from this, a data input bus line system is adopted for less power consumption. With this system, data inputs from LSI function only when appropriate data are sent.

The following shows the a full screen signal electrode data inputs and the driver LSI chip select functions.

First, when the driver LSI at the left is selected to send 80-dot data (20CP2), the right side driver close to it is selected. This action continues until the data have been sent to the driver LSI at the right. This process takes place at the same time with the signal electrode drive LSI for both screen sectors.

In this manner, data for both screen sectors are supplied through the 4-bit bus line one at a time.

Because this graphic display unit does not have the internal refresh RAM, it is necessary to supply the data and its timing pulse.



NOTE: [1,2] "1" represent the first vertical dot and "2" the second horizontal dot.

Fig. 5-5 Dot chart of Display Area

2. Static LCD

2-1. Structure

This unit is equipped with a 5-segment ON State LCD for display of key functions.

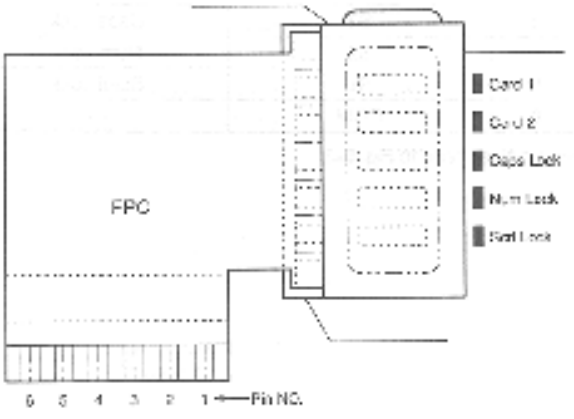


Fig. 5-3

2-2. Specifications

1) Drive conditions

Power voltage: 5V
Duty: Static

2) Max. rating

AC applying voltage: 10V (within 1 hour)
DC applying voltage: 3.5V (within 100 hours)
Storage temperature: –20 – 60°C
Operating temperature: 0 – 40°C

3) Electric, optical characteristics

No.	Item		Symbol	Temperature °C		Standard values			Unit
						Min.	Typ.	Max.	
1	Vth voltage		Vop	0	Vth2				V
					Vth1		2.50	2.70	
				25	Vth2				
					Vth1		2.30	2.50	
				40	Vth2				
					Vth1		2.10	2.30	
2	Response time		Tr	Low temperature					ms
				0			60	90	
				25			20	30	
			Tf	Low temperature					
				0			90	140	
				25			30	50	
3	Frame frequency		fF				64		Hz
4	Capacity		C	25			1.0	1.5	nF
5	View range	Forward/Backward	θ	φ = 0°		50		80	DEG
		Right/Left	θ	φ = 270°		60		120	
6	AC current value		IAC	25			1.2	3.1	μA
7	Contrast ratio			25			5		

2-3. Interfacing signals

Pin No.	Signal name	Segment
1	S5	CARD1
2	S4	CARD2
3	S3	Caps Lock
4	S2	Num Lock
5	S1	Scrol Lock
6	COM	—

For pin Nos., refer to Fig .5-6.