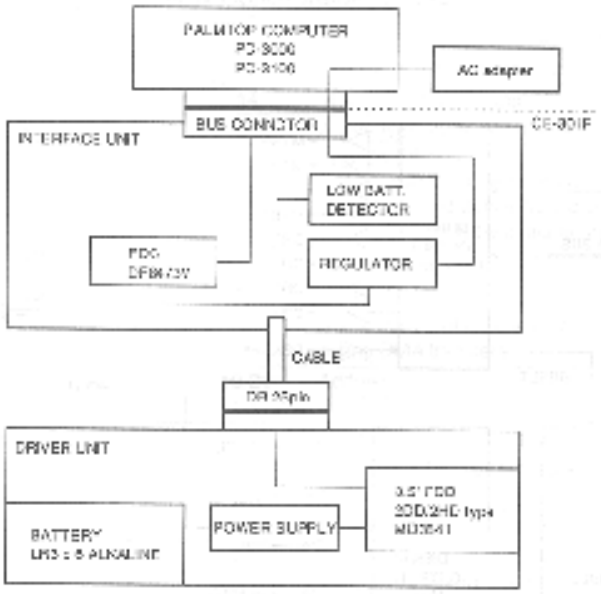
CHAPTER 8. 3.5" FDD unit (CE-301F)

1. General description

The CE-301F is an external 3.5" 2HD/2DD FDD unit for use with the palm-top computer PC-3000/3100.
It is composed of the I/F circuit and the drive unit connected with a cable each other. The cable can be separated from the drive unit side. (25 pin D-SUB)
The I/F circuit is connected to the bus connector of the main body (Fixed manually with a screw.)
It can be driven by batteries in the drive unit. (Alkali LR6 batteries × 6).
It can be driven by AC adaptor connected to the main body.
The tilt mechanism is provided in the drive unit side. (Bezel is lifted.)

2. System configuration



3. Specifications

(1) I/F section

FDC	: NS DP8473V (IBM AT/XT compatible)
Host I/F	: 90 pin connector FDC address decode circuit Power control circuit (AC adaptor selection, battery low battery detection)
Drive connection	: Direct connection of 25 pin D-SUB connector cable (Cable length: 400mm)
External dimensions	: 88 × 60 × 20mm, excluding cable and projection

(2) Drive unit section

FDD	: CANON MD-3541 3.5" 2HD/2DD type
Power circuit	: Battery driven DC-DC circuit
Power source	: Built-in LR6 alkali batteries × 6, or AC adaptor connected to the main body. (AC adaptor input has the priority. When there is no batteries in the main body, AC adaptor is used.)
Tilt	: Bezel side is lifted about 5°.
External dimensions	: 124 × 222 × 31.5 mm
Environment	: (Operation) Temperature: 10°C – 35°C, Humidity: 20% – 80% (Without condensation) (Storage) Temperature: –20°C – 55°C, Humidity: 10% – 90% (Without condensation)
Weight	: Approx. 1.0kg

4. FDC (DP8473)

4-1. General Description

This controller is a full featured floppy disk controller that is software compatible with the μPD765A, but also includes many additional hardware and software enhancements. These enhancements include additional logic specifically required for an IBM® PC, PC-XT®, PC-AT® or PS/2® design. This controller incorporates a precision analog data separator, that includes a self trimming delay line and VCO. Up to three external filters are switched automatically depending on the data rate selected. This provides optimal performance at the standard PC data rates of 250/300 kb/s, and 500 kb/s. It also enables optimum performance at 1 Mb/s (MFM). These features combine to provide the lowest possible PLL bandwidth, with the greatest lock range, and hence the widest window margin.
This controller includes write precompensation circuitry. A shift register is used to provide a fixed 125 ns early-late precompensation for all tracks at 500k/300k/250 kb/s (83 ns for 1 MB/s), or a precompensation value that scales with the data rate. 83 ns/125 ns/208 ns/250 ns for data rates of 1.0M/500k/300k/250 kb/s respectively.
Specifically to support the PC-AT and PC-XT design, the Floppy Disk Controller PLUS-2 includes address decode for the A0-A2 address lines, the motor/drive select register, data rate register for selecting 250/300/500 kb/s, Disk Changed status, dual speed spindle motor control, low write current and DMA/interrupt sharing logic. The controller also supports direct connection to the μP bus via internal 12 mA buffers. The controller also can be connected directly to the disk drive via internal open drain high drive outputs, and Schmitt inputs.
In addition to this logic the DP8473 includes many features to ease design of higher performance drives and future controller upgrades. These include 1.0 Mb/s data rate, extended track range to 4096, implied seeking, working Scan Commands, motor control timing, both standard IBM formats as well as Sony 3.5" (ISO) formats, and other enhancements. This device is available in a 52 pin Plastic Chip Carrier, and in a 48 pin Dual-In-Line package.

4-2. Features

- Fully μPD756A and IBM-RISS compatible
- Integrates all PCXT®, PCAT®, and most PS/2® Logic
  - On chip 24 MHz Crystal Oscillator
  - DMA enable logic
  - IBM compatible address decode of A0 – A2
  - 12 mA μP bus interface buffers
  - 48 mA floppy drive interface buffers
  - Data rate and drive control registers
- Precision analog data separator
  - Self calibrating PLL and delay line
  - Automatically chooses one of three filters
  - Intelligent read algorithm
- Two pin programmable precompensation modes
- Other enhancements
  - Up to 1 Mb/s data rate
  - Implied seek up to 4000 tracks
  - IBM or ISO formatting
- Low power CMOS, with power down mode

4-3. Connection Diagrams

Plastic Leaded Chip Carrier

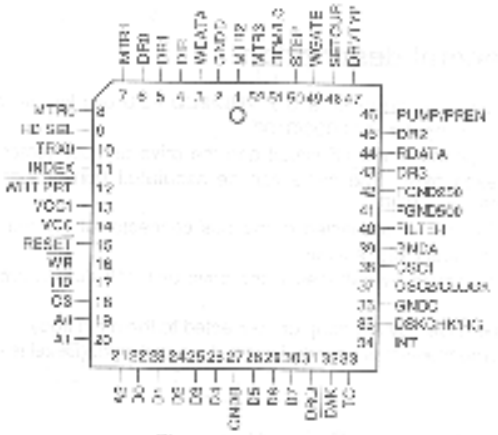
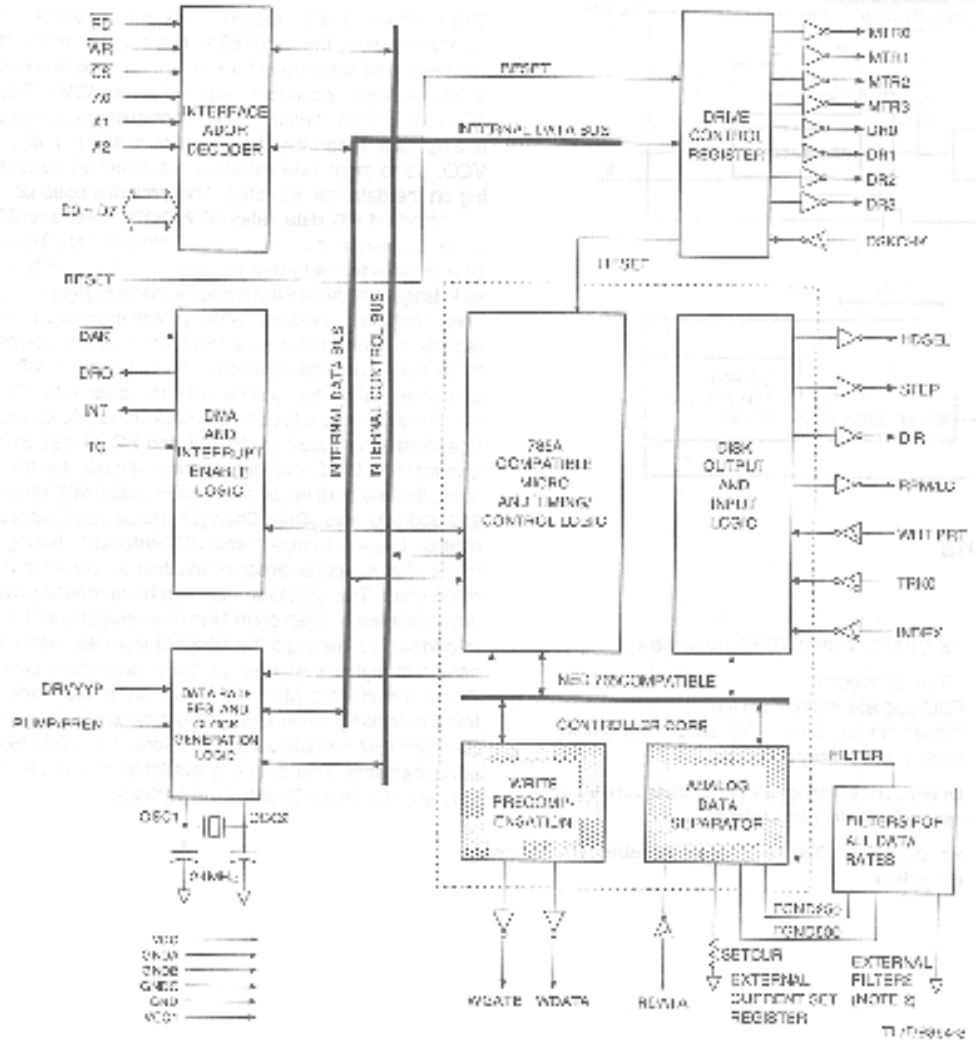


Fig. 8-2 Top View
Order Number DP8473V
See NS Package Number V52A

4-4. Block Diagram



Note 1: The MTR2, MTR3, DR2, and DR3 are not available on the 48 pin DIP (DP8473N, J) versions.
Note 2: See Figure 4 for filter description.
Note 3: Total transistor count is 29,700 (approx).

Fig. 8-3 DP8473 Functional Block Diagram

4-5. Pin Descriptions

Symbo	DP8473 PDC	Functior
MTR2	1	This is an active low motor enable line for drive 2, which is controlled by the Drive Control register. This is a high drive open drain output.
GNDD	2	This pin is the digital ground for the disk interface output drivers.
WDATA	3	This is the active low open drain write precompensated serial data to be written onto the selected disk drive. This is a high drive open drain output.
DIR	4	This output determines the direction of the head movement (low = step in, high = step out). When in the write or read modes, this output will be high. This is a high drive open drain output.
DR1	5	This is an active low drive select line for drive 1 that is controlled by the Drive Control register bits D0, D1. The Drive Select bit is ANDed with the Motor Enable of the same number. This is a high drive open drain output.
DR0	6	This is an active low drive select similar to DR1 line except for drive 0.
MTR1	7	This is an active low motor enable line for drive 1. Similar to MTR2.
MTR0	8	This is an active low motor enable line for drive 0. Similar to MTR2.
HD SEL	9	This output determines which disk drive head is active. Low = Head 1, Open (high) = Head 0. This is a high drive open drain output.
TRK0	10	This active low Schmitt input tells the controller that the head is at track zero of the selected disk drive.
INDEX	11	This active low Schmitt input signal the beginning of a track.
WRT PRT	12	This active low Schmitt input indicates that the disk is write protected. Any command that writes to that disk drive is inhibited when a disk is write protected.
V_{CCA}	13	This pin is the 5V supply for the analog data separator circuitry.
V_{CC}	14	This pin in the 5V supply for the digital circuitry.
RESET	15	Active high input that resets the controller to the idle state, and resets all the output lines to the disk drive to their disabled state. The Drive Control register is reset to 00. The Data Rate register is set to 250 kb/s. The Specify command registers are not affected. The Mode Command registers are set to the default values. Reset should be held active during power up. To prevent glitches activating the reset sequence, a small capacitor (1000 pF) should be attached to this pin.
$\overline{WR}$	16	Active low input to signal a write from the microprocessor to the controller.
$\overline{RD}$	17	Active low input to signal a read from the controller to the microprocessor.
$\overline{CS}$	18	Active low input to enable the RD and $\overline{WR}$ inputs. Not required during DMA transfers. This should be held high during DMA transfers.
A0, A1, A2	19-21	Address lines from the microprocessor. This determines which registers the microprocessor is accessing as shown in Table IV in the Register Description Section. Don't care during DMA transfers.
D0-D4	22-26	Bi-directional data lines to the microprocessor. These are the lower 5 bits and have buffered 12 mA outputs.
GNDR	27	This pin is the digital ground for the 12 mA microprocessor interface buffers. This includes D-D7, INT, and DRQ.
D5-D7	28-30	Bi-directional data lines to the microprocessor. These upper 3 bits have buffered 12 mA outputs.
DRQ	31	Active high output to signal the DMA controller that a data transfer is needed. This signal is enabled when D3 of the Drive Control Register is set.
$\overline{DAK}$	32	Active low input to acknowledge the DMA request and enable the $\overline{RD}$ and $\overline{WR}$ inputs. This signal is enabled when D3 of the Drive Control Register is set.
TC	33	Active high input to indicate the termination of a DMA transfer. This signal is enabled when the DMA Acknowledge pin active.
INT	34	Active high output to signal that an operation requires the attention of the microprocessor. The action required depends on the current function of the controller. This signal is enabled when D3 of the Drive Control Register is set.
DSKCHG/FG	35	This latched Schmitt input signal is inverted and routed to D7 of the data bus and is read when address xx7H is enabled. When the RG bit in the Mode Command is set, this pin functions as a Read Gate signal that when low forces the data separator to lock to the crystal, and when high it locks to data for diagnostic purposes.
GNDC	36	This pin is the digital ground for the controller's digital logic, including all internal registers, micro-engine, etc.
OSC2/CLOCK	37	One side of the external 24 MHz crystal is attached here. If a crystal is not used, a TTL or CMOS compatible clock is connected to this pin.
OSC1	38	One side of an external 24 MHz crystal is attached here. This pin is tied low if an external clock is used.
GNDA	39	This pin is the analog ground for the data separator, including all the PLLs, and delay lines.
FILTER	40	This pin is the output of the charge pump and the input to the VCO. One or more filters are attached between this pin and the GNDA, FGND250 and FGND500 pins.
FGND500	41	This pin connects the PLL filter for 500k(MFM)/250k(FM) bps to ground. This is a low impedance open drain output.
FGND250	42	This pin connects the PLL filter for 250k(MFM)/125k(FM) bps or 300k(MFM)/150k(FM) bps to ground. This is a low impedance open drain output.
DR3	43	This is the same as DR0 except for drive 3.

Symbol	DP8473 PQC	Function
RDATA	44	The active low raw data read from the disk is connected here. This is a Shmit input.
DR2	45	This is the same as DR0 except for drive 2.
PUMP/PREN	46	When the PU bit is set in Mode Command this pin is an output that indicates when the charge pump is making a correction. Otherwise this pin is an input that sets the precomp mode as shown in Table VI. If pin is configured as PUMP, PREN is assumed high.
DRV TYP	47	This is an input used by the controller to enable the 300 kb/s mode. This enables the uses of floppy drives with either dual or single speed spindle motors. For dual speed spindle motors, this pin is tied low. When low, and 300 kb/s data rate is selected in the data rate register, the PLL actually uses 250 kb/s. This pin is tied high for single speed spindle motor drives (standard AT drive). When this pin is high and 300 kb/s is selected 300 kb/s is used. (See also RPM/LC pin).
SETCUR	48	An external resistor connected from this pin to analog ground programs the amount of charge pump current that drives the external filters. The PLL Filter Design section shows how to determine the values.
WGATE	49	This active low open drain high drive output enables the write circuitry of the selected disk drive. This output has been designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.
STEP	50	This active low open drain high drive output will produce a pulse at a software programmable rate to move the head during a seek operation.
RPM/LC	51	This high drive open drain output pin has two functions based on the selection of the DRVTYP pin. 1. When using a dual speed spindle motor floppy drive (DRVTYP pin low) this output is used to select the spindle motor speed, either 300 RPM or 360 RPM. In this mode this output goes low when 250/300 kb/data rate is chosen in the data register, an high when 500 kb/s is chosen. 2. When using a single speed spindle motor floppy drive (DRVTYP pin high), this pin indicates when to reduce the write current to the drive. This output is high for high density media (when 500 kb/s is chosen).
MTR3	52	This is an active low motor enable line for drive 3.

5. High speed switching regulator controller (TL1454C)

5-1. General description

The TL1454C is PWM system high-speed switching regulator control IC. The reference voltage circuit of 1.25V and triangular waveform oscillation circuit which allows high frequency oscillation allow perfect synchronization of two circuits. The output circuit is of totem pole output suitable for high speed operation and step-down/inverting output and step-up output are available. Its power consumption is low and operates on a low voltage, being suitable for portable unit power source.

5-2. Features

- Wide range of power voltage: 3.6V ~ 20V
- Low current consumption: 3.0mA (Typ)
- Built-in malfunction prevention circuit at low voltage
- Highly precise reference voltage source
- Timer system output short protection circuit (Built-in)
- Wide range of operating oscillation frequency allows high frequency oscillation: 50kHz ~ 2MHz
- Adjustment of stop period is possible for all duty range.

5-3. Pin arrangement (Top view)

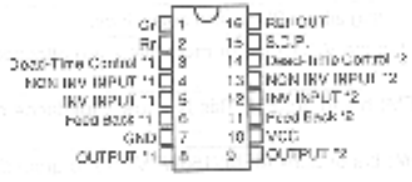
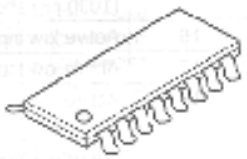


Fig. 5-4

5-4. Package external view



NS package 16 pin

Fig. 5-5

5-5. Block diagram

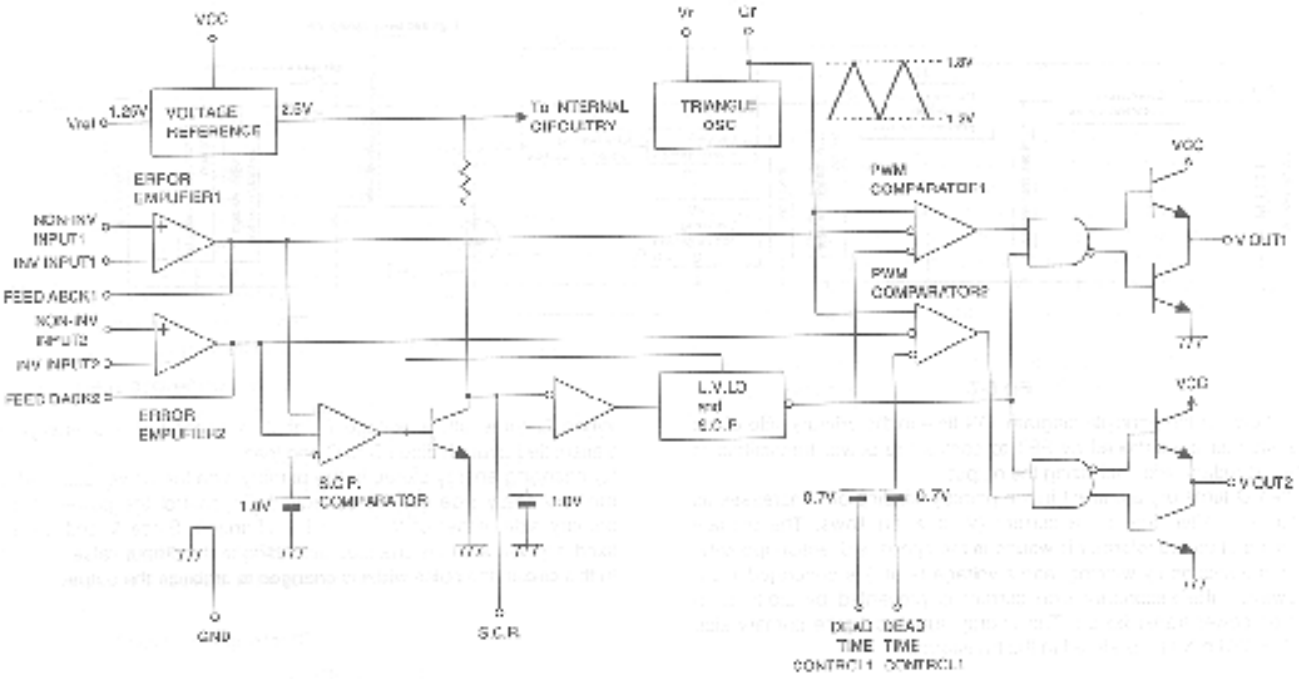


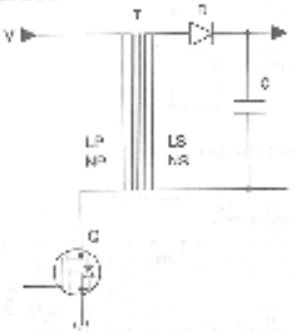
Fig. 3-6

6. DC-DC power supply

6-1. Outline of DC-DC

The DC-DC convertor section employs the PWM flyback convertor system. Six alkali manganese batteries (LR06) generate +5V output. The output can be turned on/off by external control.

6-2. Composition



The DC-DC convertor is composed of the overcurrent protection circuit, the noise filter section, the reverse polarity protection section, the overcurrent protection section, the input filter section, the ON/OFF control section, the overheating protection section, the switching control section, the snubber section, the switching FET section, the high frequency transformer, the high speed rectifying diode, the output voltage detection section, the overvoltage protection section, and the output filter section.

6-3. Operational description

Power from the batteries is passed through the overcurrent prevention section and the noise filter section where external noises are removed, and the overvoltage protection circuit to the input filter.
This power is converted into intermittent current in the switching section and transmitted through the flyback transformer to the secondary side and stabilized.

To keep the output at a constant level according to the load condition, switching duty (pulse width) is varied and transmitted power is controlled.

6-4. Outline of PWM flyback DC-DC

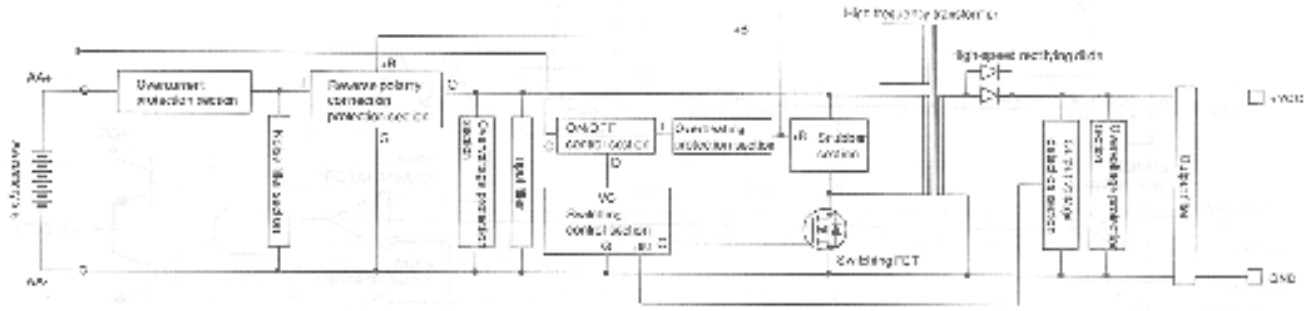
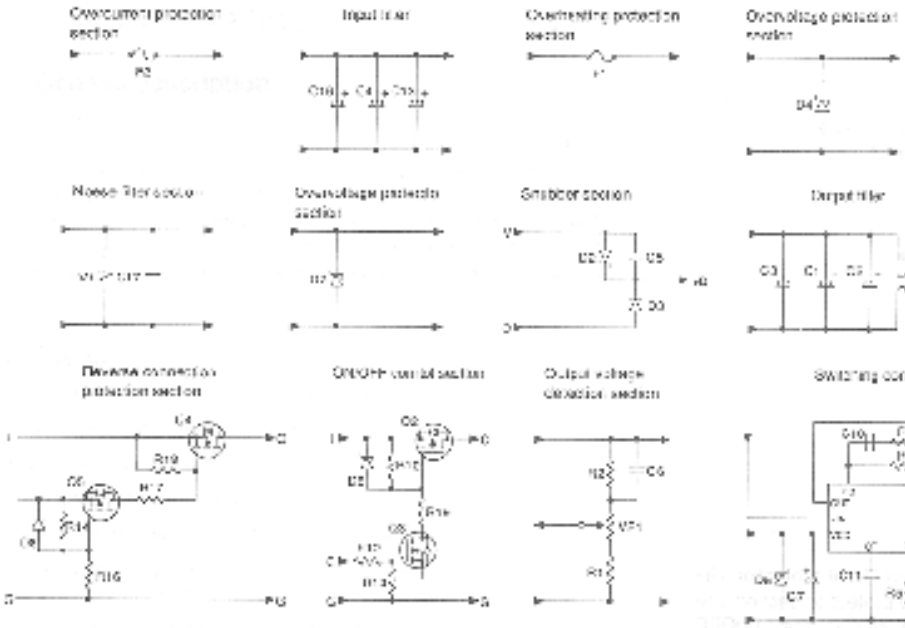


Fig 6-7

As shown in the principle diagram, ON time in the primary side of the transformer is controlled by FET to control the power transmitted to the secondary side, stabilizing the output.
When Q turns on, a current in the primary winding of T increases as V/Lp × t. After time t1, a current (V/Lp × t1) flows. The primary winding of the transformer is wound in the opposite direction (polarity) with the secondary winding, and a voltage (+ at .) is generated in Ls. However, the secondary side current is prevented by diode D to inhibit power transmission. The energy supplied to the primary side (1/2 × V/Lp × t^2) is stored in the transformer.
When Q turns off, a voltage (– at .) is generated and energy is transmitted through diode D to C and load.
By changing energy stored in the primary side,the power supplied to the secondary side can be controlled. To control the power in the primary side, either of V, Lp, or t is changed. Since V and Lp are fixed, t (pulse width) is changed according to the output value.
In this circuit the pulse width is changed to stabilize the output.

6-5. Operational description of each section

(1) Overcurrent protection circuit



This circuit is composed of the fuse. When an overcurrent flows because of breakdown of parts, the fuse is blown off to protect the system.
This part is the important part and be sure to use the specified one only.

(2) Noise filter section

This section is composed of varistor V1 and capacitor C17. The function is to absorb spike noises from external circuits and protect the system.

(3) Reverse polarity connection protection section

This section is composed of PchFET Q5, NchFET Q4, resistors R18, R19, R17, R14, and zener diode D8. When AA battery is inserted reversely, Q5 and Q4 are reversely biased to be turned off. Therefore no reverse voltage appears in and after Q4 to protect the system. D8 is a zener diode which prevents an overvoltage from being applied to Q5 gate. It serves as the gate protection diode. The resistors are used for bias to FET.

(4) Input filter section

This section is composed of capacitors C16, C4, and C13.
It absorbs noised in the switching section and decreases the impedance in the power line to stabilize the operations. Since a large ripple current flows through this section, capacitors of large allowable ripple current are used. (Organic semiconductor capacitors)

(5) Overvoltage protection section (Input)

This section is composed of zener diode D7. When the input voltage exceeds the zener voltage (12V), D7 conducts and F2 is blown off to protect the system.

(6) ON/OFF control section

This section is composed of NchFET Q3, PchFET Q2, zener diode D6, and resistors R12, R13, R9, and R10.

By supplying logic level signals to the control pin, ON/OFF control of the output can be performed. (C pin: Control pin)

When a voltage of 2.6V or more is applied to C pin, Q3 is turned on to pull –Q2 gate to GND and Q2 is turned on to supply power to the switching control section, which starts DC-DC operation.

When C pin is open or at GND level, Q3 and Q2 are off and no power is supplied to the switching section.

D6 zener diode is for protection of Q2 and the resistor is for bias.

(7) Overheat protection section

This section is composed of thermal fuse F1 which is heat-connected with switching transistor Q1. When Q1 temperature rises abnormally, the fuse is blown off to cu. the power supplied to the switching section and protect the system from overheat. This fuse is also an important maintenance part, and be sure to use the specified one only.

(8) Switching control section

This section is composed of switching regulator IC U1, resistors and capacitors.

U1:	Switching regulator IC
R5:	Switching frequency setting resistor
C11:	Switching frequency setting capacitor
C14:	Short protection circuit operation start time setting capacitor
R6/R11:	Dead time (Max. duty) setting resistors
C12:	Software start setting capacitor
R4/R3/R7:	Gain and frequency correction resistors
C10:	Frequency correction resistor
C13:	Reference voltage bypass capacitor
C7:	Bypass capacitor for power source
D5:	IC protection zener diode

Outline of operation: The voltage from the output voltage detection section is compared with the reference voltage and the pulse duty applied to switching FET Q5 is changed so that the output voltage is constant.

(9) Snubber section

This section is composed of capacitor C5, diode D3, and zener diode D8.

Since the primary side and the secondary side of the transistor are not connected 100% perfectly, a leakage inductance is generated. When energy is stored to primary side inducrance Lp by switching FET ON, some energy is also stored to leakage inductance Ll. When switching FET is turned off, energy stored in Lp is transmitted to Ls, but energy stored in leakage inductance is not transmitted. This will generate a high voltage in winding Np. To protect switching FET from this high voltage, the current is rectified by D3 and stored in C5 and dissipated in D2 as the form of heat. Some part of energy stored in this section is used to power the switching control section.

(10) Output voltage detection section

This section is composed of resistors R2 and R1, semi-fixed resistor VR1, and capacitor C6.

The output voltage is dropped by R2, R1, and VR1 to return to the switching section.

By adjusting VR1, the output voltage can be changed. C6 is the capacitor for phase compensation to stabilize the control system.

(11) Overvoltage protection circuit (Output side)

This section is composed of zener diode D4. When the output voltage exceeds D4 zener voltage, D4 conducts to operate the short-circuit prevention circuit. As a result, the output is stopped and the system is protected against an overvoltage and breakage.

(12) Output filter section

This section is composed of electrolytic capacitors C3, C1, C2 and C9, ceramic capacitor C9, and common mode choke coil L1.

C3, C1, and C2 function to smooth the switched current to convert into an DC current. Since a large ripple current flows through the capacitors, organic semiconductor capacitors of low impedance of high frequency are used. Since normal aluminum electrolytic capacitors will generate a large quantity of heat to exhaust their lives quickly and will also increase the output ripple voltage, they cannot be used.

L1 is common mode choke coil which prevents against switching noise and reduces output spike noises. C8 and C9 are used to absorb normal mode noises.