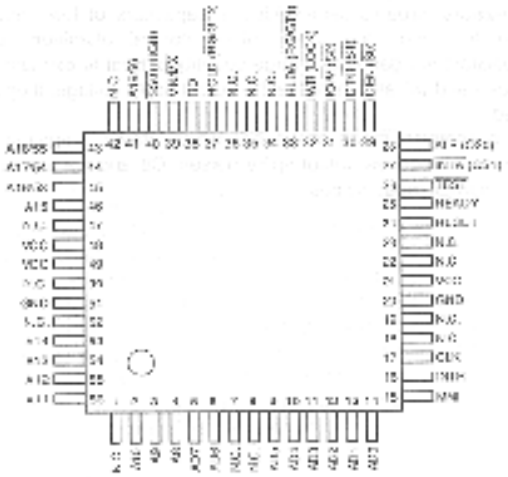
CHAPTER 9. DESCRIPTION OF LSI'S

1. CPU (MSM80C88A-10GS)

1-1. Pin configuration



1-2. Pin description

SYMBOL	NAME	I/O	FUNCTION
AD0 – AD7	ADDRESS DATA BUS	Input/ Output	These lines are the multiplexed address and data bus. These are the address bus at T1 cycle and the data bus at T2, T3, TW and T4 cycle. T2, T3, TW and T4 cycle. These lines are high impedance during interrupt acknowledge and hold acknowledge.
A8 – A15	ADDRESS BUS	Output	These lines are the address bus bits 8 thru 15 at all cycles. These lines do not have to be latched by an ALE signal. These lines are high impedance during interrupt acknowledge and hold acknowledge.
A16/S3, A17/S4, A18/S5, A19/S6	ADDRESS/ STATUS	Output	These are the four most significant address as at the T1 cycle. Accessing I/O port address, these are low at T1 Cycles. These lines are Status lines at the T2, T3, TW and T4 Cycle. S6 indicate interrupt enable flat. S3 and S4 are encoded as shown. S3 | S4 | Characteristics 0 | 0 | Alternate Data 1 | 0 | Stack 0 | 1 | Code or None 1 | 1 | Data These lines are high impedance during hold acknowledge.
RD	READ	Output	This lines indicates that the CPU is in a memory or I/O read cycle. This line is the read strobe signal when the CPU reads data from a memory or I/O device. This line is active low. This line is high impedance during hold acknowledge.
READY	READY	Input	This line indicates to the CPU that an addressed memory or I/O device is ready to read or write. This line is active high. If the setup and hold time are out of specification, an illegal operation will occur.
INTR	INTERRUPT REQUEST	Input	This line is a level triggered interrupt request signal which is sampled during the last clock cycle of instruction and string manipulations. It can be internally masked by software. This signal is active high and internally synchronized.

SYMBOL	NAME	I/O	FUNCTION
$\overline{TEST}$	TEST	Input	This line is examined by a "WAIT" instruction. When $\overline{TEST}$ is high, the CPU enters an idle cycle. When $\overline{TEST}$ is low, the CPU exits an idle cycle.
NMI	NON MASKABLE INTERRUPT	Input	This line causes a type 2 interrupt. NMI is not maskable. This signal is internally synchronized and needs a 2 clock cycle pulse width.
RESET	RESET	Input	This signal causes the CPU to initialize immediately. This signal is active high and must be at least four clock cycles.
CLK	CLOCK	Input	This signal provide the basic timing for an internal circuit.
MN/$\overline{MX}$	MINIMUM/ MAXIMUM	Input	This signal selects the CPU's operate mode. When Vcc is connected, the CPU operates in minimum mode. When GND is connected, the CPU operates in maximum mode.
Vcc	Vcc		+5V supplied
GND	GROUND		The following pin function descriptions are for maximum mode only Other pin functions are already described.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	STATUS	Output	These lines indicate bus status and they are used by the MSM82C88 Bus Controller to generate all memory and I/O access control signals. These lines are high impedance during hold acknowledge. These status lines are encoded as shown.
$\overline{RQ}$/GT0 $\overline{RQ}$/GT1	REQUEST/ GRAND	Input/Output	These lines are used for Bus Request from other devices and Bus GRANT to other devices. These lines are bidirectional and active low.
$\overline{LOCK}$	LOCK	Output	This line is active low. When this line is low, other devices can not gain control of the bus. This line is high impedance during hold acknowledge.
QS0/QS1	QUEUE STATUS	Output	These are Queue Status Lines that indicate internal instruction queue status.
IO/$\overline{M}$	STATUS	Output	This line selects memory address space or I/O address space. When this line is low, the CPU selects memory address space and when it is high, the CPU selects I/O address space. This line is high impedance during hold acknowledge.
$\overline{WR}$	WRITE	Output	This line indicates that the CPU is in a memory or I/O write cycle. This line is a write strobe signal when the CPU writes data to memory or an I/O device. This line is active low. This line is high impedance during hold acknowledge.
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE	Output	This line is a read strobe signal for the interrupt acknowledge cycle. This line is active low.
ALE	ADDRESS LATCH ENABLE	Output	This line is used for latching an address into the MSM82C12 address latch it is a positive pulse and the trailing edge is used to strobe the address. This line in never floated.
DT/$\overline{R}$	DATA TRANSMIT/ RECEIVE	Output	This line is used to control the direction of the bus transceiver. When this line is high, the CPU transmits data, and when it is low, the CPU receive data. This line is high impedance during hold acknowledge.
$\overline{DEN}$	DATA ENABLE	Output	This line is used to control the output enable of the bus transceiver. This line is active low. This line is high impedance during hold acknowledge.

$\overline{S2}$	$\overline{ST}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1 (HIGH)	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

QS1	QS0	Characteristics
0 (LOW)	0	No Operation
0	1	First Byte of Op Code from Queue
1 (HIGH)	0	Empty the Queue
1	1	Subsequent Byte from Queue

The following pin function descriptions are minimum mode only. Other pin functions are already described.

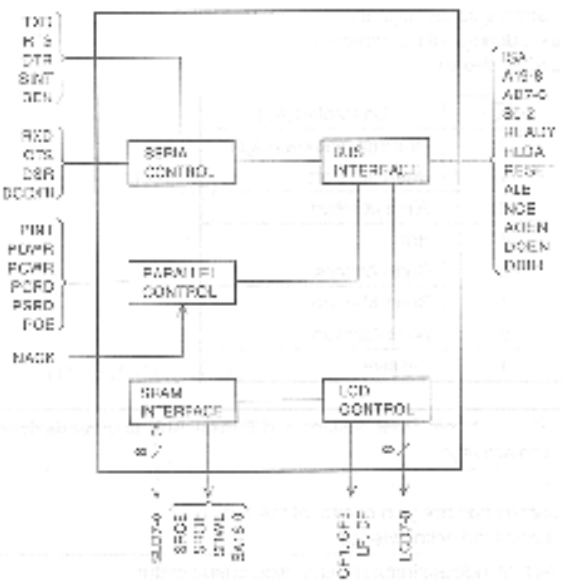
SYMBOL	NAME	I/O	FUNCTION
HOLD	HOLD REQUEST	Input	This line is used for a Bus Request from an other device. This line is active high.
HLDA	HOLD ACKNOWLEDGE	Output	This line is used for a Bus Grant to an other device.
$\overline{S0}$	STATUS	Output	This line is logically equivalent to $\overline{S0}$ in the maximum mode.

2. DVC ASIC(μPD65658)

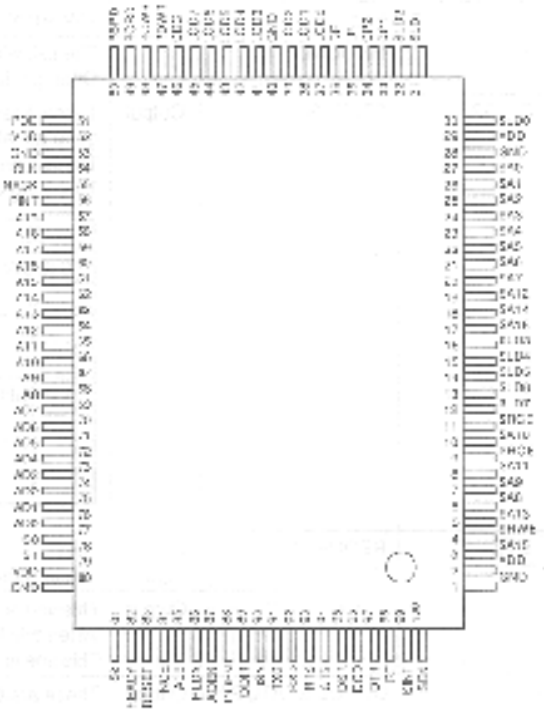
2-1. Introduction

The DVC contains a LCD controller with MDA, CGA and AT & I compatible modes, a 8250B serial controller and parallel printer port.

2-2. Block diagram



2-3. Pin configuration



2-4. Pin description

1) CPU I/F

NAME	NO.	TYPE	DESCRIPTION
ISA	1	INP	ISA bus/8086 CPU bus
A19-8	12	INP	Address
AD7-0	8	BID	Address/Data
S2-2	3	INP	CPU status/ISA IOW, IOR, MEMR Strobes
READY	1	OUT	CPU wait
HLDA	1	INP	DMA cycle in progress, (ISA AEN)
RESET	1	INP	
ALE	1	INP	
NCE	1	INP	SPC ASIC memory mapping – SA MEMW
ADEN	1	OUT	ISA Addr/Data Mux Scheme Address enable
DOEN	1	OUT	ISA Addr/Data Mux Scheme Data enable
DDIR	1	OUT	ISA Addr/Data Mux Scheme direction

(33)

2) Serial controller I/F

NAME	NO.	TYPE	DESCRIPTION
TXD	1	OUT	Transmit serial data
RXD	1	INP	Receive serial data
RTS	1	OUT	Request To Send
CTS	1	INP	Clear To Send
DSR	1	INP	Data Send Request
DCD	1	INP	Data Carrier Detect
DTR	1	OUT	Data Terminal Ready
RI	1	INP	Ring Indicator
SINT	1	OUT	Serial Controller Interrupt
SEN	1	OUT	Serial Interface Power Down

(10)

3) Parallel Printer port I/F

NAME	NO.	TYPE	DESCRIPTION
PDWR	1	OUT	Printer data write strobe
PCWR	1	OUT	Printer control write strobe
PCRD	1	OUT	Printer control read strobe
PSRD	1	OUT	Printer status read
POE	1	OUT	Printer buffer output enable
NACK	1	INP	Not printer ACK
PRINT	1	OUT	Printer port interrupt

(7)

4) SRAM I/F

NAME	NO.	TYPE	DESCRIPTION
SA16-0	17	OUT	SRAM address
SD7-0	8	BID	SRAM data/CD data
SRCE	1	OUT	SRAM Chip Enable
SROE	1	OUT	SRAM Output Enable
SRWE	1	OUT	SRAM Write Enable

(28)

5) LCD I/F

NAME	NO.	TYPE	DESCRIPTION
CP1	1	OUT	LCD line clock pulse
CP2	1	OUT	LCD pixel clock
LF	1	OUT	LCD line sync
DF	1	OUT	LCD frame toggle
LCD7-0	8	OUT	LCD data

(12)

6) OTHER I/F signals

NAME	NO.	TYPE	DESCRIPTION
CDC	1	OUT	Contrast voltage
CLK	1	INP	LCD Clock 10.00 Mhz

(2)

Total = (33) + (10) + (7) + (28) + (12) + (2) = 92

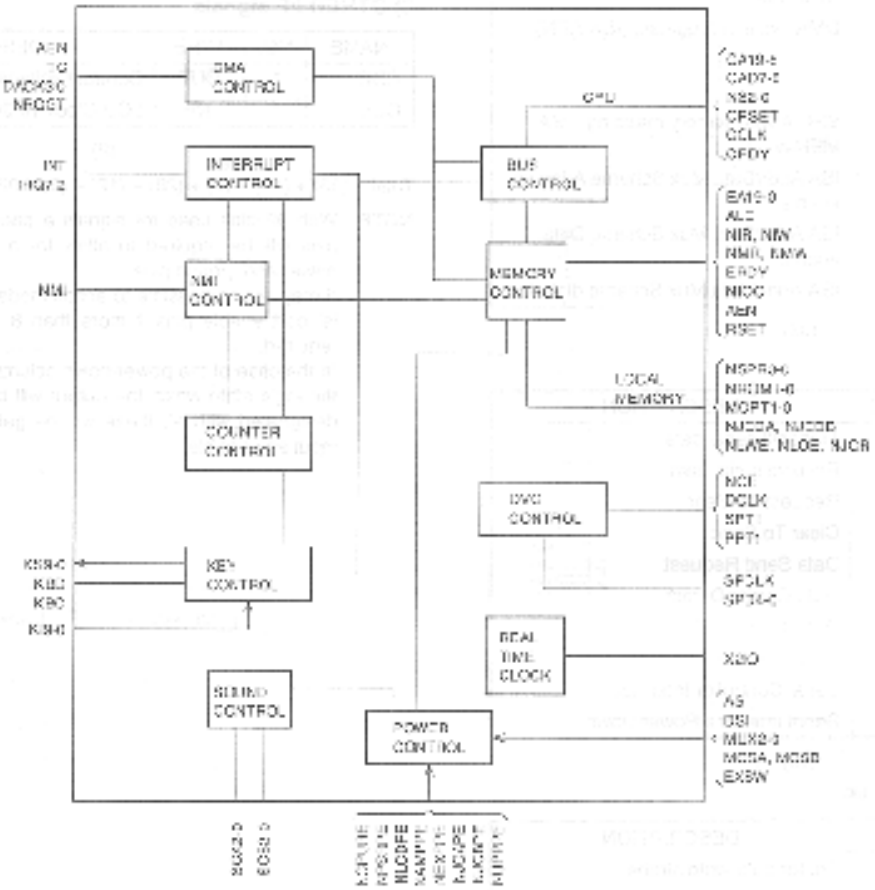
NOTE: With 92 pins used for signals a package with at least 100 pins will be required to allow for a reasonable number of power and ground pins.
It may not be possible to accommodate the serial and parallel port enable pins if more than 8 power supply pins are required.
In the case of the power-down column, the state indicated is the logic state which the output will be forced to. Inputs are designated with '-', these will be gated off as close to the input as possible.

3. SPC ASIC (TC146G68)

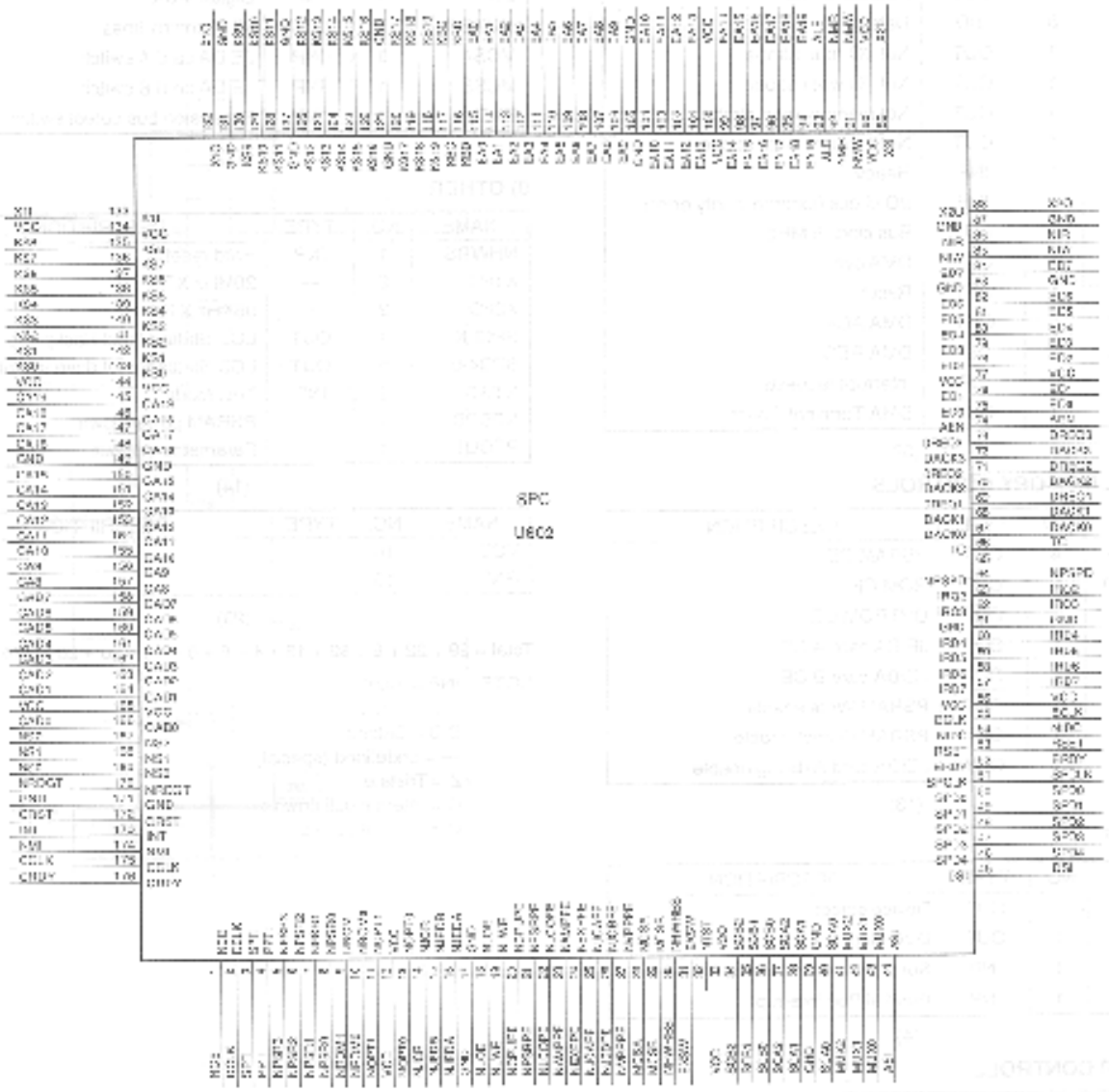
3-1. Introduction

The SPC ASIC contains all the logic needed to fully implement a PC compatible machine, in addition SPC specific logic is included.

3-2. Block diagram



3-3. Pin configuration



3-4. Pin description

1) CPU I/F

NAME	NO.	TYPE	DESCRIPTION
CA19-8	12	BID	Address
CAD7-0	8	BID	Address/Data
NS2-0	3	BID	CPU Status
NRQGT	1	BID	DMA Request/Grant
GRST	1	OUT	CPU Reset
INT	1	OUT	Interrupt
NMI	1	OUT	Non maskable interrupt
CCLK	1	OUT	Clock
CRDY	1	OUT	Ready

(29)

2) KEYBOARD

NAME	NO.	TYPE	DESCRIPTION
KS9-0	10	BID	Scan lines
KI9-0	10	INP	Sense lines
KBD	1	BID	Serial keyboard data
KBC	1	BID	Serial keyboard clock

(22)

3) SOUND

NAME	NO.	TYPE	DESCRIPTION
SCA2-0	3	OUT	Channel 1
SCB2-0	3	OUT	Channel 2

(6)

4) EXPANSION BUS

NAME	NO.	TYPE	DESCRIPTION
EA19-0	20	OUT	Address
ALE	1	OUT	Address strobe
ED7-0	8	BID	Data
NIR	1	OUT	Not I/O read strobe
NIW	1	OUT	Not I/O write strobe
NMR	1	OUT	Not memory read strobe
NMW	1	OUT	Not memory write strobe
ERDY	1	INP	Ready
NIOC	1	INP	I/O check (external parity error)
ECLK	2	OUT	Bus clock 5 MHz
AEN	1	OUT	DMA cycle
RESET	1	OUT	Reset
DACK3-0	4	OUT	DMA ACK
DREQ3-1	3	INP	DMA REQ
IRQ7-2	6	INP	Interrupt requests
TC	1	OUT	DMA Terminal Count

(52)

5) LOCAL MEMORY CONTROLS

NAME	NO.	TYPE	DESCRIPTION
NPSR3-0	4	OUT	PSRAM CE
NROM1-0	2	OUT	ROM CE
NOPT1-0	2	OUT	OPTROM CE
NJEDA	1	OUT	JEIDA card A CE
NJEDB	1	OUT	JEIDA card B CE
NLWE	1	OUT	PSRAM Write enable
NLOE	1	OUT	PSRAM Output enable
NJCR	1	OUT	JEIDA card A-B reg enable

(13)

6) DVC I/F

NAME	NO.	TYPE	DESCRIPTION
NCE	1	OUT	Device select
DCLK	1	OUT	DVC clock
SPTI	1	INP	Serial controller interrupt
PPTI	1	INP	Parallel Port interrupt

(4)

7) POWER CONTROLL

NAME	NO.	TYPE	DESCRIPTION
NCPUPE	1	OUT	CPU, ROM, Parallel Port, JEIDA Buffers
NPSRPE	1	OUT	PSRAM
NLCDPE	1	OUT	LCD
NAMPPE	1	OUT	Audio Amp
NEXPPE	1	OUT	Expansion Unit
NJCAPE	1	OUT	JEIDA card A
NJCBPE	1	OUT	JEIDA card B
NVPPPE	1	OUT	Vpp for JEIDA card B

(8)

8) SENSE LINES

NAME	NO.	TYPE	DESCRIPTION
ASI	1	INP	Level Detector
DSI	1	INP	Digital MUX
MUX2-0	3	OUT	MUX control lines
MCSA	1	INP	JEIDA card A switch
MCSB	1	INP	JEIDA card B switch
EXSW	1	INP	Expansion bus detect switch

(8)

9) OTHER

NAME	NO.	TYPE	DESCRIPTION
NHWRS	1	INP	Hard reset
X1I/O	2	—	20MHz XTL
X2I/O	2	—	96KHz XTL
SPCLK	1	OUT	LCD Status Panel Backplane
SPD4-0	5	OUT	LCD Status Panel drive signals
NTST	1	INP	Test Mode
NPSPD	1		PSRAM power down
PTOUT	1		Parametric test out

(14)

NAME	NO.	TYPE	DESCRIPTION
VCC	10		
GND	10		

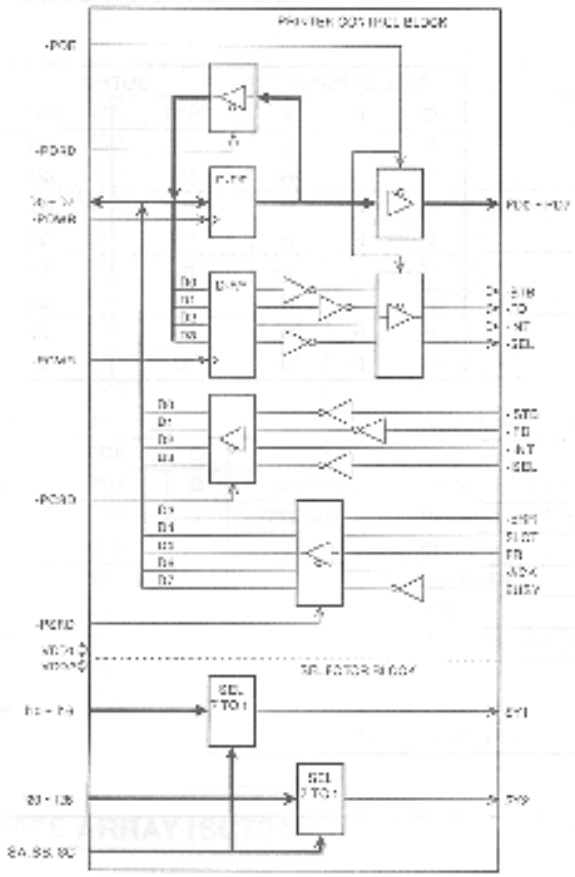
(20)

Total = 20 + 22 + 6 + 52 + 13 + 4 + 3 + 8 + 14 + 20 + 20 = 176

NOTE: INP = Input
OUT = Output
BID = Bidirect
— = undefined (special)
Z = Tristate
D = Internal pull down
U = Internal pull up

4. STANDARDCELL (SC2060FOA)

4-1. Block diagram



4-2 Pin Description

The custom CMOS IC functions as (1) printer buffer and (2) selector. Although independent power supply systems are used in function blocks (1) and (2), VDD (1) ≥ VDD (2).

● **SC2060F0A terminals**

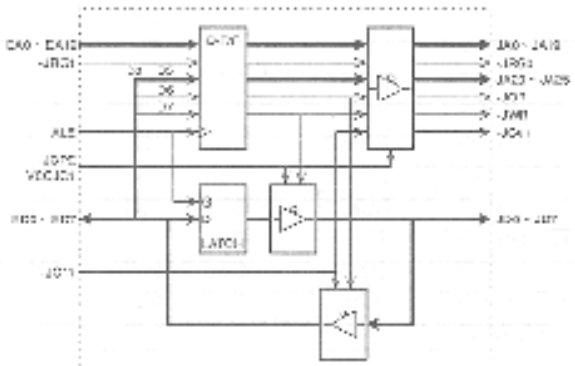
Pin No.	Signal	I/O	Buffer	Function
1	VDD2	—	—	Selector power supply
2	I10	I	CMOS Schmitt	Selector 1 input 0
3	I11	I	CMOS Schmitt	Selector 1 input 1
4	I12	I	CMOS Schmitt	Selector 1 input 2
5	VSS	—	—	GND
6	I13	I	CMOS Schmitt	Selector 1 input 3
7	I14	I	CMOS Schmitt	Selector 1 input 4
8	I15	I	CMOS Schmitt	Selector 1 input 5
9	I16	I	CMOS Schmitt	Selector 1 input 6
10	NC	—	—	Not in use
11	SA	I	CMOS Schmitt	Selector selective input A
12	SB	I	CMOS Schmitt	Selector selective input B
13	SC	I	CMOS Schmitt	Selector selective input C
14	SY1	O	Totem pole	Selector 1 selective output
15	NC	—	—	Not in use
16	VSS	—	—	GND
17	SY2	O	Totem pole	Selector 2 selective output
18	I20	I	CMOS Schmitt	Selector 2 input 0
19	I21	I	CMOS Schmitt	Selector 2 input 1
20	I22	I	CMOS Schmitt	Selector 2 input 2
21	I23	I	CMOS Schmitt	Selector 2 input 3
22	I24	I	CMOS Schmitt	Selector 2 input 4
23	I25	I	CMOS Schmitt	Selector 2 input 5
24	I26	I	CMOS Schmitt	Selector 2 input 6
25	VDD2	—	—	Selector power supply
26	VSS	—	—	GND
27	$\overline{POE}$	I	TTL	Printer output enable, active: "L"
28	PRQ	O	3-STATE	Unused
29	D0	I/O	C-MOS	CPU data 0
30	NC	—	—	Not in use
31	D1	I/O	C-MOS	CPU data 1
32	D2	I/O	C-MOS	CPU data 2
33	D3	I/O	C-MOS	CPU data 3
34	VDD1	—	—	Printer power supply
35	NC	—	—	Not in use
36	VSS	—	—	GND
37	D4	I/O	C-MOS	CPU data 4
38	D5	I/O	C-MOS	CPU data 5
39	D6	I/O	C-MOS	CPU data 6
40	D7	I/O	C-MOS	CPU data 7
41	$\overline{PDWR}$	I	TTL	Printer data write signal (data latched with)
42	$\overline{PSRD}$	I	TTL	Printer status read signal (active: "L")
43	$\overline{PCWR}$	I	TTL	Printer control write signal (data latched with)
44	$\overline{PCRD}$	I	TTL	Printer control read signal (active: "L")
45	VSS	—	—	GND
46	VDD1	—	—	Printer power supply
47	$\overline{PDRD}$	I	TTL	Unused (printer data read signal)
48	$\overline{RESET}$	I	TTL Schmitt	Printer control signal clear
49	$\overline{ISTB}$	I	TTL Schmitt	Printer control $\overline{STROBE}$ signal monitor input
50	NC	—	—	Not in use
51	$\overline{STB}$	O	Open drain	Printer control $\overline{STROBE}$ signal output
52	$\overline{IFD}$	I	TTL Schmitt	Printer control $\overline{AUTO\ FD}$ signal monitor input

SELECT INPUT			OUTPUT	
C	B	A	SY1	SY2
L	L	L	I10	I20
L	L	H	I11	I21
L	H	L	I12	I22
L	H	H	I13	I23
H	L	L	I14	I24
H	L	H	I15	I25
H	H	L	I16	I26
H	H	H	L	L

Pin No.	Signal	I/O	Buffer	Function
53	$\overline{FD}$	O	Open drain	Printer control -AUTO FD signal output
54	VDD*	—	—	Printer power supply
55	NC	—	—	Not in use
56	VSS	—	—	GND
57	$\overline{INIT}$	I	TTL Schmit.	Printer control $\overline{INIT}$ signal monitor input
58	$\overline{INIT}$	O	Open drain	Printer control $\overline{INIT}$ signal output
59	$\overline{SEL}$	I	TTL Schmit.	Printer control $\overline{SELECT\ IN}$ signal input
60	$\overline{SEL}$	O	Open drain	Printer control $\overline{SELECT\ IN}$ signal output
61	PD0	O	3-STATE	Printer data 0 output
62	PD1	O	3-STATE	Printer data 1 output
63	VDD*	—	—	Printer power supply
64	VSS	—	—	GND
65	PD2	O	3-STATE	Printer data 2 output
66	PD3	O	3-STATE	Printer data 3 output
67	PD4	O	3-STATE	Printer data 4 output
68	PD5	O	3-STATE	Printer data 5 output
69	VSS	—	—	GND
70	NC	—	—	Not in use
71	PD6	O	3-STATE	Printer data 6 output
72	PD7	O	3-STATE	Printer data 7 output
73	$\overline{ERR}$	I	TTL Schmit.	Printer status $\overline{ERROR}$ signal input
74	VDD*	—	—	Printer power supply
75	NC	—	—	Not in use
76	VSS	—	—	GND
77	SLCT	I	TTL Schmit.	Printer status $\overline{SLCT}$ input
78	PE	I	TTL Schmit.	Printer status PE input
79	$\overline{ACK}$	I	TTL Schmit.	Printer status $\overline{ACK}$ input
80	BUSY	I	TTL Schmit.	Printer status BUSY input

5. GATE ARRAY (SC7220F4E)

5-1. Block diagram



5-2. Pin Description

A custom C-MOS IC is provided for each of two IC cards as IC card interface.

Pin No.	Signal	I/O	Buffer	Function
1	VSS	—		GND
2	$\overline{OUTE}$	I	CMOS Schmitt	Unused, fixed at "L"
3	EA16	I	TTL	External bus address 16
4	EA17	I	TTL	External bus address 17
5	EA18	I	TTL	External bus address 18
6	EA19	I	TTL	External bus address 19
7	$\overline{JRGI}$	I	TTL	-JRG signal input from SPC
8	$\overline{JCEI1}$	I	TTL	Card select signal input from SPC
9	NC	—	—	Not in use
10	ALE	I	TTL	ALE from SPC
11	$\overline{JCPE}$	I	CMOS Schmitt	Operation enable signal for this IC; operation enabled with "L"
12	VSS	—	—	GND
13	NC	—	—	Not in use
14	JD3	I/O	Pull down	IC card data 3
15	JD4	I/O	Pull down	IC card data 4
16	JD5	I/O	Pull down	IC card data 5
17	JD6	I/O	Pull down	IC card data 6
18	JD7	I/O	Pull down	IC card data 7
19	$\overline{WDE}$	I	TTL	Data write signal from SPC to IC card
20	$\overline{JCEO1}$	O	3-STATE	IC card chip select output
21	JA10	O	3-STATE	IC card address 10
22	$\overline{JOE}$	O	3-STATE	IC card data read signal
23	JA11	O	3-STATE	IC card address 11
24	VSS		—	GND
25	NC	—	—	Not in use
26	VDD	—		Power supply
27	JA9	O	3-STATE	IC card address 9
28	JA8	O	3-STATE	IC card address 8
29	JA13	O	3-STATE	IC card address 13
30	JA14	O	3-STATE	IC card address 14
31	JA17	O	3-STATE	IC card address 17
32	JA18	O	3-STATE	IC card address 18
33	JA19	O	3-STATE	IC card address 19
34	VSS	—	—	GND
35	JA20	O	3-STATE	IC card address 20
36	JA21	O	3-STATE	IC card address 21
37	$\overline{JWE}$	O	3-STATE	IC card write signal
38	NC	—	—	Not in use
39	JA16	O	3-STATE	IC card address 16
40	JA15	O	3-STATE	IC card address 15
41	NC	—	—	Not in use
42	JA12	O	3-STATE	IC card address 12
43	VSS	—	—	GND
44	JA22	O	3-STATE	IC card address 22
45	JA23	O	3-STATE	IC card address 23
46	JA24	O	3-STATE	IC card address 24
47	JA25	O	3-STATE	IC card address 25
48	$\overline{JRCO}$	O	3-STATE	IC card attribute memory select signal
49	$\overline{CLM}$	I	CMOS Schmitt	Test terminal, fixed at "H" or "L"
50	VDD	—	—	Power supply
51	NC	—	—	Not in use
52	VSS	—	—	GND
53	JA7	O	3-STATE	IC card address 7
54	JA6	O	3-STATE	IC card address 6

Pin No.	Signal	I/O	Buffer	Function
55	JA5	O	3-STATE	IC card address 5
56	JA4	O	3-STATE	IC card address 4
57	JA3	O	3-STATE	IC card address 3
58	JA2	O	3-STATE	IC card address 2
59	JA1	O	3-STATE	IC card address 1
60	JA0	O	3-STATE	IC card address 0
61	VSS	—	—	GND
62	JD0	I/O	Pull down	IC card data 0
63	NC	—	—	Not in use
64	JD1	I/O	Pull down	IC card data 1
65	JD2	I/O	Pull down	IC card data 2
66	MM	O	Totem pole	Unused (alternating signal output)
67	NC	—	—	Not in use
68	EA0	I	TTL	External bus address 0
69	EA1	I	TTL	External bus address 1
70	EA2	I	TTL	External bus address 2
71	EA3	I	TTL	External bus address 3
72	EA4	I	TTL	External bus address 4
73	EA5	I	TTL	External bus address 5
74	EA6	I	TTL	External bus address 6
75	VSS	—	—	GND
76	VDD	—	—	Power supply
77	CP1	I	CMOS Schmitt	Unused, fixed at "L" or "H" (LCD clock)
78	SS	I	CMOS Schmitt	Unused, fixed at "L" or "H" (LCD clock)
79	VCCJC1	I	CMOS Schmitt	Power monitor terminal for IC card
80	EA7	I	TTL	External bus address 7
81	EA8	I	TTL	External bus address 8
82	EA9	I	TTL	External bus address 9
83	EA10	I	TTL	External bus address 10
84	EA11	I	TTL	External bus address 11
85	EA12	I	TTL	External bus address 12
86	EA13	I	TTL	External bus address 13
87	EA14	I	TTL	External bus address 14
88	NC	—	—	Not in use
89	EA15	I	TTL	External bus address 15
90	VSS	—	—	GND
91	NC	—	—	Not in use
92	ED0	I/O	C-MOS	External bus data 0
93	ED1	I/O	C-MOS	External bus data 1
94	ED2	I/O	C-MOS	External bus data 2
95	ED3	I/O	C-MOS	External bus data 3
96	ED4	I/O	C-MOS	External bus data 4
97	ED5	I/O	C-MOS	External bus data 5
98	ED6	I/O	C-MOS	External bus data 6
99	ED7	I/O	C-MOS	External bus data 7
100	VDD	—	—	Power supply

6. Mask ROM (LH538100)

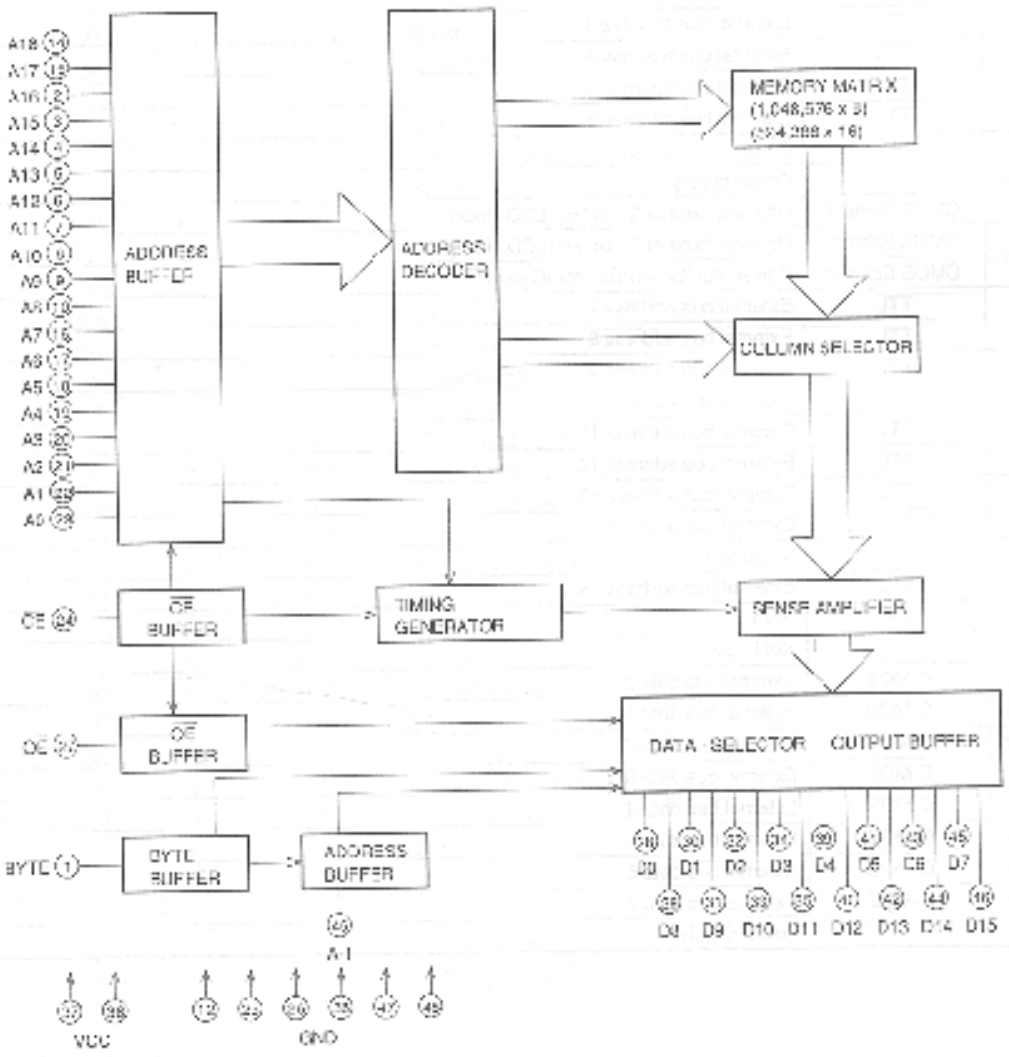
6-1. Outline

The LH538100 is an 8M-bit mask ROM manufactured by using a CMOS silicon gate process and having the following features:

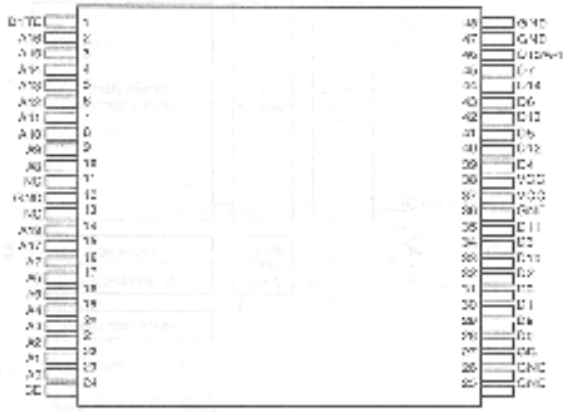
6-2. Features

- Programmable bit configuration:
  1,048,576 words × 8 bits (BYTE MODE: BYTE = V_{IL})
  524,288 words × 16 bits (WORD MODE: BYTE = V_{IH})
- Static operation (internal synchronization)
- Access time: 200 ns (max.) at Vcc = 5±10% V
- Current consumption (operation): 45 mA (max.)
- Current consumption (stand-by): 25 µA (max.) at Vcc = 5.5±20% V
- Tri-state output terminal
- Single +5 V power supply
- TTL-compatible I/O
- 48-pin, plastic TSOP

6-3. Block diagram



6-4. Pin configuration



6-5. Pin description

A-1 – A18	Address input
D0 – D15	Data output
$\overline{BYTE}$	8/16 bit (byte/word) mode-select ive input
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5 V)
GND	Ground
N.C.	Non-connection (no wire bonding)

Note: Pin 46 is:
- Used as LSB (A-1) for address input when $\overline{BYTE}$ terminal (pin 1) is set to LOW level ($\overline{BYTE}$ mode).
- Used for data output (D15) when $\overline{BYTE}$ terminal (pin 1) is set to HIGH level (WORD mode).

7. OTPROM (M5M27C101VP-15)

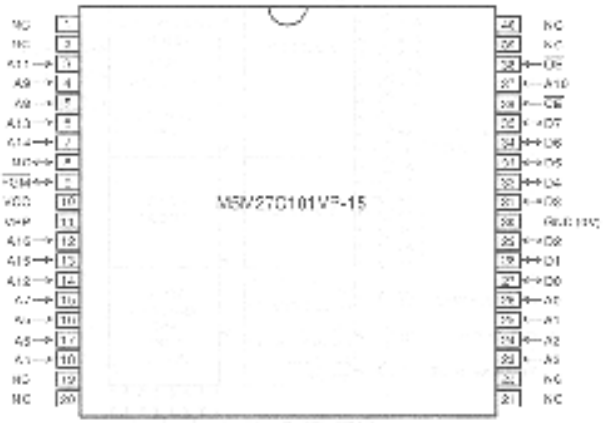
7-1. Outline

The M5M27C101VP-15 is an electrically programmable CMOS OTPROM (One-Time Programmable ROM) with a configuration of 1,048,576 bits (131,072 words × 8 bits).
The M5M27C101VP-15 is a CMOS OTPROM that is best suited for a wide range of ROM applications, including microprocessor systems. The M5M27C101VP-15 employs a EPROM (UV-erasable PROM) in a plastic package. In the EPROM, CMOS silicon gate technology is utilized for peripheral units and N channel double silicon gate technology is utilized for the memory unit.

7-2. Features

- Access time: 150 ns (max.)
- Package:
  M5M27C101VP-15: TSOP
- Static circuit
- I/O directly connectable to TTL in READ or PROGRAM mode
- Power supply:
  READ mode: 5 V single power supply
  PROGRAM mode: 12.5 V
- Programming: Byte or page programming
- JEDEC standard 32-pin DIP, PLCC
- Pin compatibility with 1M-bit EPROM (DIP, PLCC)

7-3. Pin configuration



External view

7-4. Functions

Read operation

Setting both of the $\overline{CE}$ and $\overline{OE}$ terminals to "L" and inputting address signals (using address input terminals A_0 – A_{16}) causes the stored data to be outputted from the data output terminals (D_0 – D_7). Setting either the $\overline{CE}$ or $\overline{OE}$ terminal to "H" sets the data I/O terminals to the floating status. Setting the $\overline{CE}$ terminal to "H" sets the data I/O terminals to the stand-by status (POWER DOWN mode).

Write operation

Byte programming

Setting the $\overline{CE}$ terminal to "L" and the $\overline{OE}$ terminal to "H" and applying a voltage of 12.5 V to the V_{PP} terminal activates the PROGRAM mode. The address is set with the address input terminals (A_0 – A_{16}). The data to be written is specified in 8-bit parallel with the data input terminals (D_0 – D_7). Setting the $\overline{PGM}$ terminal to "L" starts the byte programming.

Page programming

Setting the CE terminal to "H", the $\overline{OE}$ terminal to "L", and the $\overline{PGM}$ terminal to "H" and applying a voltage of 12.5 V to the V_{PP} terminal activates the PAGE DATA LATCH mode. Four different addresses are set with the address input terminals (A_0 – A_{16}). Four different data (total 4 bytes), each corresponding to the individual addresses, is specified in 8-bit parallel with the data input terminals (D_0 – D_7). At this point, the 4 bytes of data are latched in the PROM. Setting the $\overline{OE}$ terminal to "H" and the $\overline{PGM}$ terminal to "L" starts the page programming (synchronous 4-byte write operation).

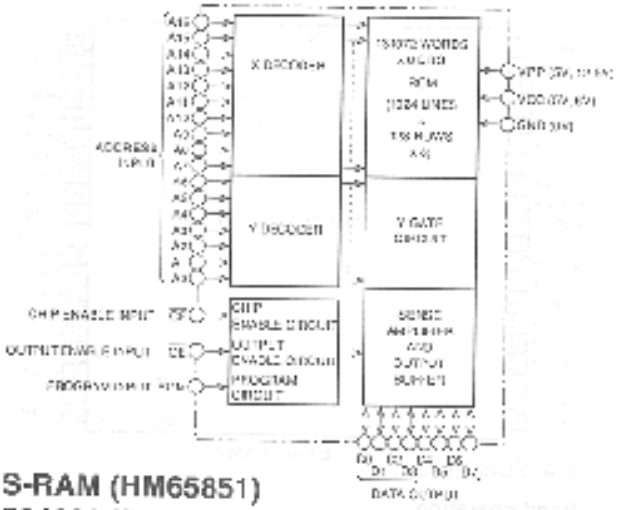
Erase operation

Data cannot be erased since the plastic package does not have a UV transmission window.

Precautions for handling

Great care should be taken to avoid an overvoltage, especially upon power-up, although a high voltage is required for write operation.

7-5. Block diagram



8. S-RAM (HM65851)
524288-Word × 8-Bit High Speed Pseudo Static RAM

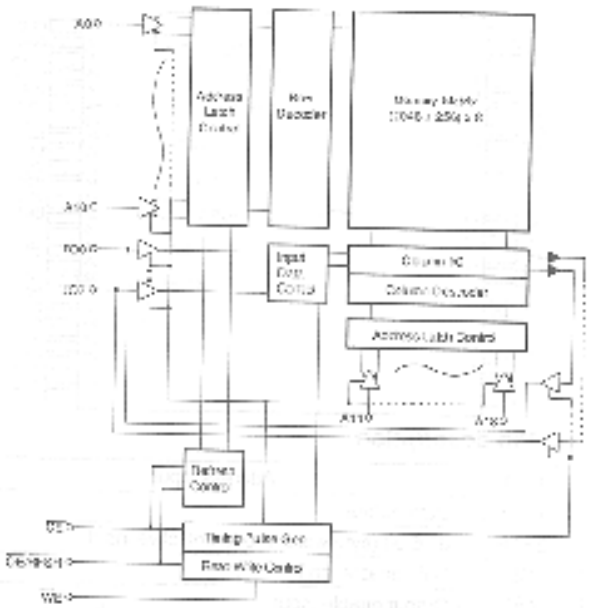
8-1. Features

- Single 5V (±10%)
- High speed
  - Access time
    CE access time: 80/100/120 ns
  - Cycle time
    Random read/write cycle time:
    160/180/210 ns
    Low power
  - 250 mW typ active
  - 350 µW typ standby (L-version)
  - 200 µW typ standby (LL-version)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
- Non multiplexed address
- 2048 refresh cycles /32 ms
- Refresh functions
  - L-version: Address refresh
    LL-version: Automatic refresh
    Self refresh
  - D-version: Address refresh
    Automatic refresh

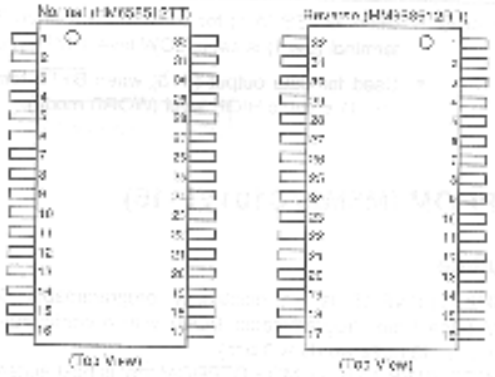
8-2. Pin Description

Pin name	Function
A0 – A18	Address
I/O0 – IO7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$/RFSH	Output enable/refresh
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

8-3. Block Diagram



8-4. Pin Configuration of HM658512TT/RR



Pin No.	Pin Name
1	A18
2	A16
3	A14
4	A12
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1

Pin No.	Pin Name
12	A0
13	I/O0
14	I/O1
15	I/O2
16	VSS
17	I/O3
18	I/O4
19	I/O5
20	I/O6
21	I/O7
22	$\overline{CE}$

Pin No.	Pin Name
23	A10
24	$\overline{OE}$/RFSH
25	A11
26	A9
27	A8
28	A13
29	$\overline{WE}$
30	A17
31	A15
32	VCC

Symbol	Function
A0 – A18	Address Inputs
I/O0 – I/O7	Data Input/Output
CE	Chip Enable
$\overline{OE}$/RFSH	Output Enable/Refresh
$\overline{WE}$	Write Enable
VCC	Power Supply
VSS	Ground

9. VRAM (M5M51008VP-12L)

9-1. Outline

Manufactured with a silicon gate CMOS process, the M5M51008VP-12L is an asynchronous static RAM with a configuration of 131,072 words × 8 bits which can operate with a single 5 V power supply.
The M5M51008VP-12L supports two types of chip select signals; the signal S_1 for memory expansion and the signal $\overline{S_2}$ for battery back-up. It also supports the output enable signal ($\overline{OE}$) for eliminating I/O data contention.
The M5M51008VP-12L is suitable for high-density surface mounting with half the surface mounting area and less than half the thickness against conventional small out-line packages.

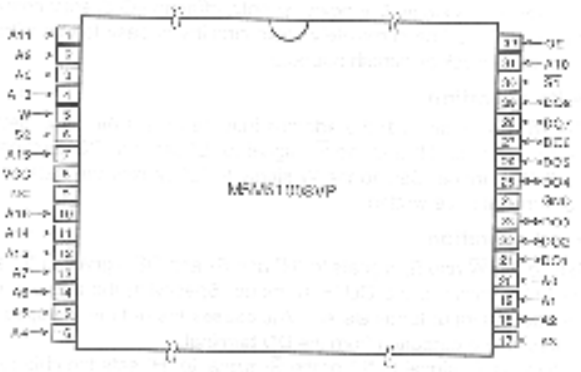
9-2. Features

- 5 V single power supply
- No external clock and refresh operation required.
- Data can be maintained with supply voltage of 2 V.
- I/O directly connectable with TTL
- Tri-state output permitting connection to OR gates
- Chip select signal for easy memory expansion
- $\overline{OE}$ input eliminating data contention on I/O bus
- Data terminal used as both an input and output terminal
- Low current consumption in stand-by status: 1.0 μA (standard value)

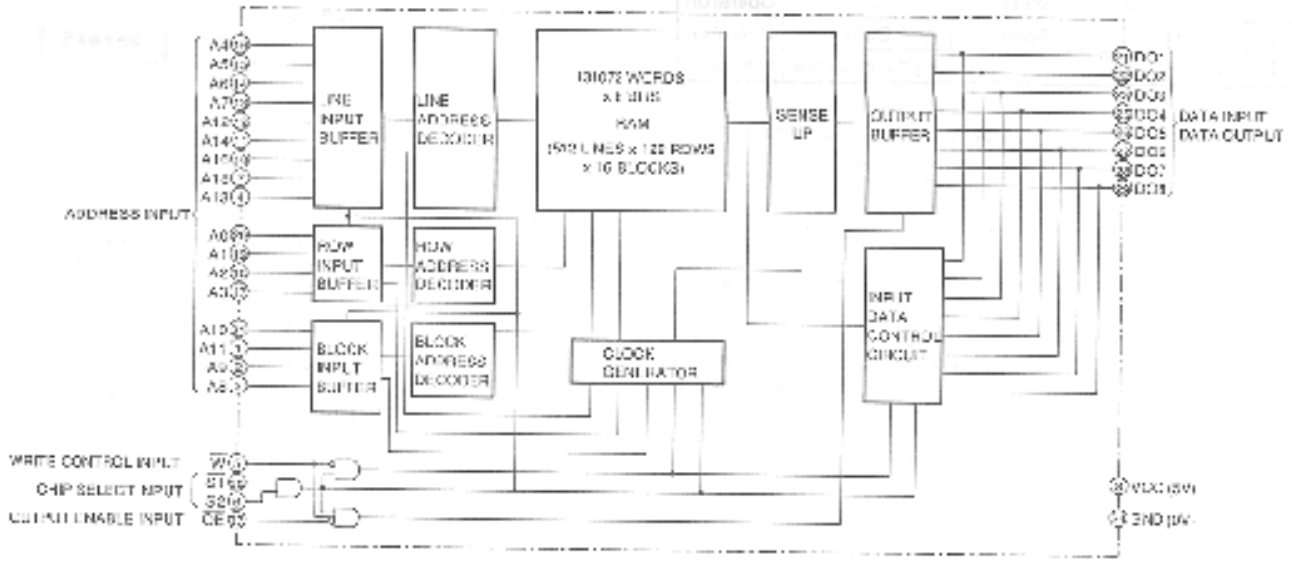
Applications

Battery drive, small storage with a battery back up unit

9-3. Pin configuration



9-4. Block diagram



9-5. Outline

The M5M51008VP-12L with a configuration of 131,072 words × 8 bits operates with a single 5 V power supply, offering I/O directly connectable with TTL. The completely static circuitry is easy to use without an external clock or refresh operation.

Write operation

The address is set with the address input terminals A_0 - A_{16}. Setting the S_2 signal to "H" and the $\overline{S_1}$ signal to "L" sets the DQ terminal to the INPUT mode. Setting the $\overline{W}$ signal to "L" causes the data at the DQ terminal to be written.

Read operation

Setting the $\overline{W}$ and S_2 signals to "H" and $\overline{S_1}$ and $\overline{OE}$ signals to "L" sets the DQ terminal to the OUTPUT mode. Specifying the address with the address input terminals A_0 - A_{16} causes the data in the specified address to be outputted from the DQ terminal.

Setting the S_2 signal to "L" or the $\overline{S_1}$ signal to "H" sets the chip to the non selective status where no read/write operation can be performed. At this point, all the outputs are in the floating status (high impedance status), where connection can be established with OR gates on other chips.

Setting the $\overline{OE}$ signal to "H" sets all the outputs to the floating status. When the I/O bus method is employed, setting the $\overline{OE}$ signal to "H" during write operation can eliminate I/O data contention.

Setting the $\overline{S_1}$ signal to V_{CC} or setting the S_2 signal to GND sets all the terminals to the stand-by status. In this status, where the M5M51008VP-12L requires only a small amount of supply current (max. 1 µA), the stored data can be maintained with a supply voltage of 2 V, thus allowing battery back-up at power failure or power down in non selective status.

Function Table

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non-selective	High impedance	Stand-by
H	X	X	X	Non-selective	High impedance	Stand-by
L	H	L	X	Write	D_{IN}	Operation
L	H	H	L	Read	D_{OUT}	Operation
L	H	H	H		High impedance	Operation