

PART 2: HARDWARE

1. General Information

The PC-3000 is an ultra-compact palmtop computer with integral keyboard, screen and memory card drives. It consists of the following components as standard:

- Main board.
Microprocessor, read-only memory (ROM), random access memory (RAM) and input/output (I/O) interfaces.
- Liquid crystal display (LCD) unit.
A large-capacity LCD with 640x200 pixel configuration. Adjustable tilt feature for better visibility.
- Two PCMCIA-specification memory card drives, conforming with Revision 1 of the specification.
- Power supply unit
- Integral keyboard.
- Speaker.
- Serial input/output (SIO) connector for RS-232C interface, via optional serial adaptor.
- Parallel input/output connector for Centronics-type printer, via optional parallel cable adaptor.
- Expansion connector to accept external expansion options for the PC-3000.
- AC adaptor connector.

9. Principles Of Operation

9.1 Introduction

This chapter describes the basic PC-3000 functions, focusing on the interaction between functional units and blocks and some characteristic circuit operations. Details of each block are contained in subsequent chapters.

9.2 Microprocessor

The PC-3000 uses the an MSM80C38A mpu (10 MHz version). This is a CMOS version of the standard 8088 processor, and is operated in maximum mode.

9.2.1 Clock

The processor operates at a master clock frequency of 10 MHz, derived from a 20 MHz oscillator. To reduce average power consumption, the gap between successive bus cycles is controlled by the SPC ASIC (CPCG register), which can vary the gap between 0 and 31 clock periods (0 to 3.1 microseconds). In effect, this varies the average clock speed between 10 and approximately 1 MHz.

The clock can also be stopped by the SPC ASIC, by clearing bit 7 of register CCNTR or PCNTR. An interrupt can set the bits, causing the clock to restart.

9.2.2 Minimum/maximum mode

The processor operates in maximum mode.

9.3 ROM

The PC-3000 contains a 1024 KByte (128 K x 8) MASK ROM and a 128 KByte OTPROM (one-time programmable ROM).

The ROM contains the following:

- * Initialization: BIOS cpu reset software. This provides the system start-up sequence after a power on or system reset. (A system reset also carries out the Power On Self Test (POST) described in chapter 6.)
- * BIOS (basic input/output system): Supports I/O devices, provides extensive extended BIOS services and a bootstrap loader for DOS.
- * Drive C: The applications and utilities built into the PC-3000, including SETUP, which enables the user to set up or update system modes and parameters with the SETUP key on the keyboard.
- * ROM Library: Support for the application programs.

9.4 RAM

The PC-3000 is fitted with two types of RAM device: PSRAM and SRAM.

psRAM (pseudo-static RAM) is refreshed using distributed refresh mode while the CPU is powered. A refresh cycle occurs every 15.13 microseconds. When the CPU is powered down, the PSRAM is held in self-refresh mode.

between two and four 512 KByte (512 K x 8) PSRAM devices may be fitted. psRAM is used for system memory, drive E and LIM EMS.

sRAM (static RAM) is powered at all times, from the AA batteries or lithium battery. A single 128 KByte (128 K x 8) SRAM device is fitted and is used for vital configuration data, video data, character fonts and drive D.

The processor can address 1 MByte of (logical) memory. The PC-3000 memory mapping hardware divides this area into 64 16KByte pages each of which has an associated mapping register (read/write). 2KByte (SRAM) and 4KByte (PSRAM) segments of RAM pages may also be individually write-protected. This means that the memory map is extremely flexible.

Memory mapping is used to implement a number of features, including LIM EMS 4.0 (expanded memory) and PCMCIA memory card access.

9.5 Memory Cards

The PC-3000 has two memory card drives which conform with PCMCIA specification release 1. Card insertion is detected by the card connector, which generates the MCDA or MCDB interrupt.

The memory card is accessed by using the memory mapping facilities.

Card ejection is detected using a mechanical switch, which generates the MCSA and MCSB interrupts. Removing a card generates the MCDA or MCDB interrupt, which causes the BIOS to turn off the power to the appropriate card connector.

9.6 Interrupts

The PC-3000 uses two levels of interrupt:

High priority - connected to the NMI pin of the processor.

Low priority - connected to the M8259 interrupt controller. This prioritizes the interrupts into 8 further levels, according to their source.

9.6.1 NMI Interrupts

There are two types hardware which can produce NMIs on PC-3000: IBM PC-compatible (I/O bus input check) and PC-3000 specific (such as power management and keyboard) devices.

If the NMI is not PC-3000 specific, the NMI vector is read from 00008..0000BH as usual. If the NMI is PC-3000 specific, the NMI vector is read from the system configuration registers NMI08..NMI0B.

NMIs can be enabled or disabled by setting the NMI mask (I/O register 0A0H). Individual NMI sources may also be enabled or disabled by writing to the appropriate bits of the SISE register. To disable all PC-3000 specific NMIs, clear bit 7 of the SISE register.

The NMIs are as follows:

Name	Source	Cleared by
ICCHK	I/O check on expansion bus	Write M8255 P85
KINT	Keyboard matrix	Read SCR
EXPI	Expansion unit switch	Read MIR
AABL1	AA battery level	Read PSIR
AABLO	AA battery level	Read PSIR
L1BL	Lithium cell level	Read PSIR
EXBL1	Expansion battery level	Read PSIR
EXBLO	Expansion battery level	Read PSIR
MABL	Memory card A battery level	Read PSIR
MSBL	Memory card B battery level	Read PSIR
ACPNR	AC power level	Read PSIR
RTCINT	Real time clock	Read RTI
TICI	OTC tick timer	Read TKI
TIMI	OTC timer	Read TMI
SPCA	Activity detector	Read ACM
PATR	Address trap	Read ATR2
KBPD	Keyboard power down register	Read SCR
MCWPA	Memory card A write protect	Read MIR
MCWPS	Memory card B write protect	Read MIR
MCD A	Memory card A detect	Read MIR
MCSB	Memory card B detect	Read MIR
MAVI	Memory access violation	Read MAV2
WINT	Keyboard wake-up	Read SISR
MCSA	Memory card A switch	Read MIR
MCSB	Memory card B switch	Read MIR
EXSW	Expansion unit switch	Read MIR
SXEI	Serial keyboard enabled (not used)	Read SISR

9.6.2 Other Interrupts

The M8259A PIC supports the following eight levels of interrupt:

Level	Source
0 (high)	M8253 PIT OUT0
1	Keyboard receive logic
2	On expansion bus
3	On expansion bus (or secondary serial controller)
4	On expansion bus (or primary serial controller)
5	On expansion bus
6	On expansion bus
7 (low)	On expansion bus (or parallel port)

9.7 Direct Memory Access (DMA)

The PC-3000 supports four DMA channels via the M8237A DMA controller, which has additional page registers to extend its addressing range to 1 MByte.

These channels are used as follows:

Channel	Used for
0 1 2 3	Latched M8253 OUT 1 (refreshing PSRAM) Available on expansion bus [1] Available on expansion bus [2] Available on expansion bus [3]

Notes:

- [1] Normally used by an SDLC serial controller on an IBM PC, if fitted.
- [2] Normally used by a floppy disk controller on an IBM PC, if fitted.
- [3] Normally used by a hard disk controller on an IBM PC, if fitted.

The extra page registers are as follows:

Address	Page register
81H	Page register 2, channel 2
82H	Page register 3, channel 3
83H	Page register 1, channel 1 and 0

bits 3 to 0 of the page register represent the extra address lines (A19 to A16) required to access 1 MByte. Bits 7 to 4 are ignored.

9.8 System Expansion

The PC-3000 supports the following standard I/O devices and I/O ports:

- * Two memory card drives
- * Liquid crystal display
- * Keyboard
- * Serial port (RS-232C)
- * Parallel port (Centronics)
- * Speaker

The unit may be extended by connecting an expansion unit.

9.9 Power Management

9.9.1 Power generation

The PC-3000 has three distinct power sources: AA batteries, AC adaptor and a Lithium cell. The AA batteries are the main power source unless the AC adaptor is connected. If the main power source fails (e.g. the AA batteries are being changed), the Lithium battery is used to power the two ASICs, SRAM and PSRAM, although it only provides power to the PSRAM for 3 minutes. The Lithium battery does not provide enough power to turn on the PC-3000.

The main supply is +5V, with all other voltages derived from this under the control of the SPC ASIC:

- * The -VEE supply is the contrast voltage for the LCD display, which may range from 0 to -16V. The level is controlled by the DVC ASIC LCD contrast controller. It is only generated while the LCD is turned on.
- * The VPP supply is a +12V supply used to program Flash Memory PCMCIA cards. It is only generated when requested by programming the ROMP register.

9.9.2 Power monitoring

The status of all the PC-3000 power supplies can be monitored by reading the power status register, PSIS:

Bit	Signal	Description
-----	--------	-------------

7	AABL1	If set, AA batteries low
6	AABL0	If set, AA batteries flat or removed
5	L1BL	If set, Lithium battery flat
4	EUBL1	If set, expansion unit supply low
3	EUBL0	If set, expansion unit supply flat
2	MCABL	If set, memory card A batteries low
1	MC3BL	If set, memory card B batteries low
0	EXTPWR	If set, external power supply low

The PSINT interrupt is generated if any of these signals goes high, if the corresponding bit in the power source mask register (PSIE) is set.

9.9.3 Power control

By writing to the SPC ASIC's PCNTR and DVC ASIC's PMEN registers, the BIOS can conserve power by turning off unnecessary devices, stopping the CPU clock or powering down the PC-3000. If the CPU clock is stopped, it will be restarted by the next interrupt from the keyboard (key press) or timer (system clock tick). Since stopping the clock also removes power to the PSRAM, you should not use this option in application programs.

The PCNTR register is bit-significant:

Bit	Controls
07	CPU power
06	CPU and PSRAM power
05	Expansion unit power
04	Automatic shut-down disable (see note 2)
03	LCD power
02	Audio amp power
01	Parallel port buffers
00	Serial port buffers

Notes:

- Setting the bit to 1 enables power; resetting it to 0 disables power.
- When bit 4 is set (1), if the main power is lost the ASIC will automatically power down by setting all bits other than 6 to 0. If bit 4 is reset (0), the BIOS must detect and handle power loss.

10. System Information

10.1 Main Memory Map

FFFF	
F8000	The BIOS (and XBIOS)
F0000	
E8000	RLI page frame (64K)
E0000	
D8000	APPS page frame
D0000	
C8000	CCM page frame
C0000	ROM extensions
C3000	BIOS and XBIOS data
C0000	CGA video buffer
B8000	HDA video buffer
B0000	
A8000	EMM page frame (64K)
A0000	
	TPA
00400	BIOS data area
00000	Interrupt vectors

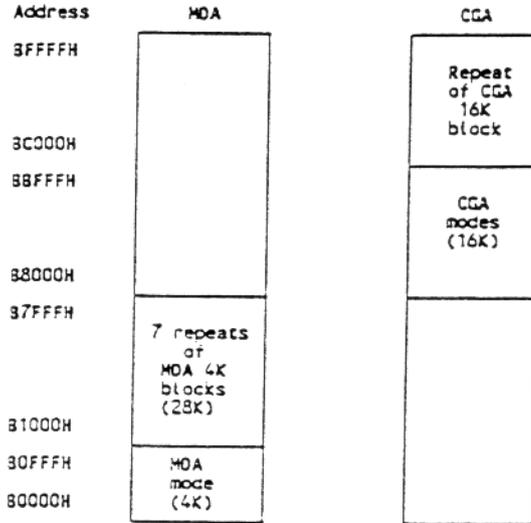
KEY:

BIOS	Basic Input/Output System
XBIOS	Extended BIOS
RLI	ROM Library interface
APPS	Built-in applications
CCM	Credit Card Memory
CGA	Colour Graphics Adaptor
HDA	Monochrome Display Adaptor
EMM	Expanded Memory Manager
TPA	Transient Program Area

For details of the BIOS, extended BIOS and interrupt vectors, see "The BIOS" (chapter 2).

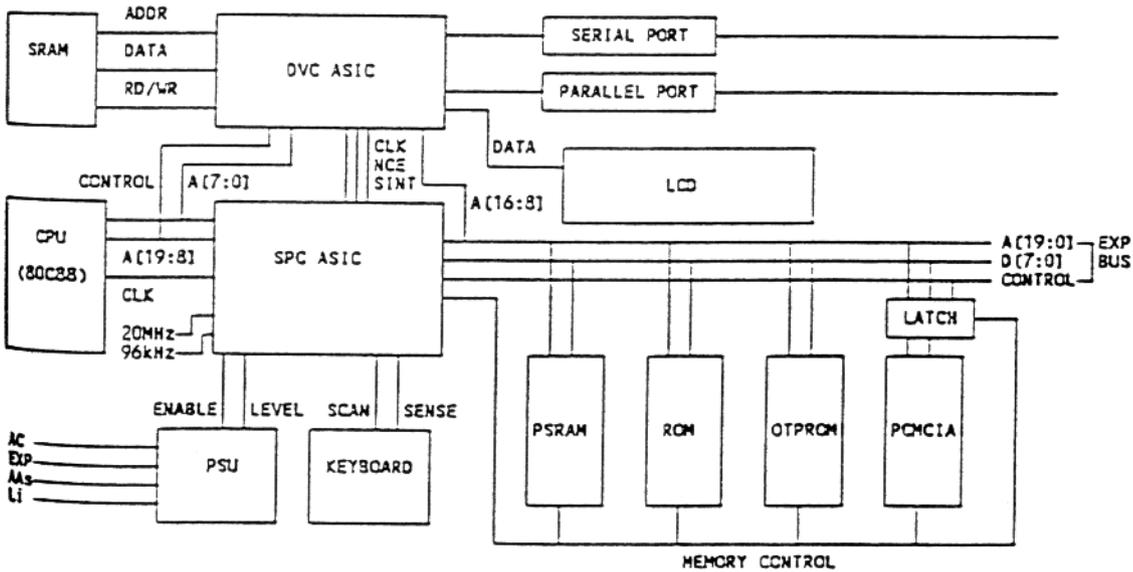
10.2 Display Memory Map

The display RAM is used as follows in the various display modes supported:



The memory organisation in each mode is as standard for these display adaptors.

10.3 System Block Diagram



10.4 I/O Address Map

The PC-3000 uses the following IBM-compatible I/O addresses. For details of the non-standard I/O, see "The SPC ASIC" (section 11.2) and "The DVC ASIC" (section 11.3).

Address	Device input	Device output
000..00F 010..01F	M8237A DMA controller **	M8237A DMA controller **
020..021 022..03F	M8259A Interrupt controller **	M8259A interrupt controller **
040..043 044..05F	M8253 PIT controller **	M8253 PIT controller **
060 061 062 063..07F	** M8255 port B ** **	M8255 port A M8255 port B M8255 port C **
080 081 082 083 084..09F	** DMA page registers 2 DMA page registers 3 DMA page registers 0 & 1 **	** ** ** ** **
0A0	NMI mask control bit	**
278 279 27A 27B..F	Printer data latch *** Printer control latch **	Printer data latch [1] Printer status [1] Printer control latch [1] **
2F8..F	M8250B serial controller	M8250B serial controller [2]
378 379 37A 37B..F	Printer data latch *** Printer control latch **	Printer data latch [1] Printer status [1] Printer control latch [1] **
380, 382 384, 386 381, 383 385, 387 388 389 38A 38B 38C 38D 38E 38F	MDA 6845 address register MDA 6845 data register MDA control register ** MDA status ** Printer data latch ** Printer control latch **	** [3] ** [3] ** [3] ** [3] MDA status [3] ** [3] Printer data latch [1] Printer status [1] Printer control latch [1] **
3D0, 3D2 3D4, 3D6 3D1, 3D3 3D5, 3D7 3D8 3D9 3DA 3DB 3DC 3DD 3DE 3DF	CGA 6845 address register CGA 6845 data register CGA mode control CGA colour select ** Clear light pen latch Set light pen latch ** ATT register **	** [3] CGA 6845 data register [3] ** [3] ** [3] CGA status register [3] ** [3] ** [3] ** [3] ATT register [4] ** [3]
3F8..F	M8250B serial controller	M8250B serial controller [2]
0400	SPC I/O Key register	[5]

Notes:

43 ** Due to partial decoding of addresses, do not use these addresses.

- [1] The printer port may be configured to appear at its primary address of 378..37F, its secondary address of 278..27F, or the MDA printer port address of 3BC..3BF. It may also be disabled.
- [2] The serial port may be configured to appear at its primary address of 3F8..3FF, or its second address of 2F8..2FF. It may also be disabled.
- [3] The LCD controller may be configured to appear as a CGA/AT&T emulation at address 3D0..3DF or as an MDA emulation at address 3B0..3BB. It may also be disabled.
- [4] The ATT register only appears if AT&T mode is selected, which is not used on the PC-3000.

With the exception of address 8400, addresses above 3FF normally wrap around, to map to the range 000..3FF. However, if the ASIC control registers are unlocked (by writing 44H to address 8400H), this address wrapping is disabled.

Accesses to devices within the SPC ASIC do not appear on the expansion bus, except for the NMI mask register.

10.5 Character Sets

There are two character sets. The ASCII characters, codes 0 to 127, are the same in both character sets:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
0		␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣
20	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣	␣
40	()	*	+	,	-	.	/	0	1	2	3	4	5	6	7	8	9	:	;
60	<	=	>	?	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
80	P	Q	R	S	T	U	U	U	X	Y	Z	[\]	^	_	`	a	b	c
100	d	e	f	g	h	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w
120	x	y	z	{		}	~	␣												

The remaining characters differ somewhat. In the default character set, they look like this:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19				
120													ç	ü	é	â	ä	à	á	ç	è	ë	è	ï
140	î	ì	ñ	ñ	é	æ	æ	ô	ö	ò	û	ù	ÿ	ÿ	U	ç	ç	ç	ç	ç	ç	ç	ç	ç
160	á	í	ó	ú	ñ	ñ	ª	ª	¿	¿	½	¼	¿	¿	¿	¿	¿	¿	¿	¿	¿	¿	¿	
180	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	†	
200	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	
220	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	
240	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	ª	

The Scandinavian character set differs in a number of characters, as indicated by double boxes in this table:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
120																				
140																				
160																				
180																				
200																				
220																				
240																				

Note that there are also two alternative thicknesses of each character set, which can be toggled by pressing Fn-F6 if Popup is installed and .

11. Main Board Unit

11.1 Processor [sharp]

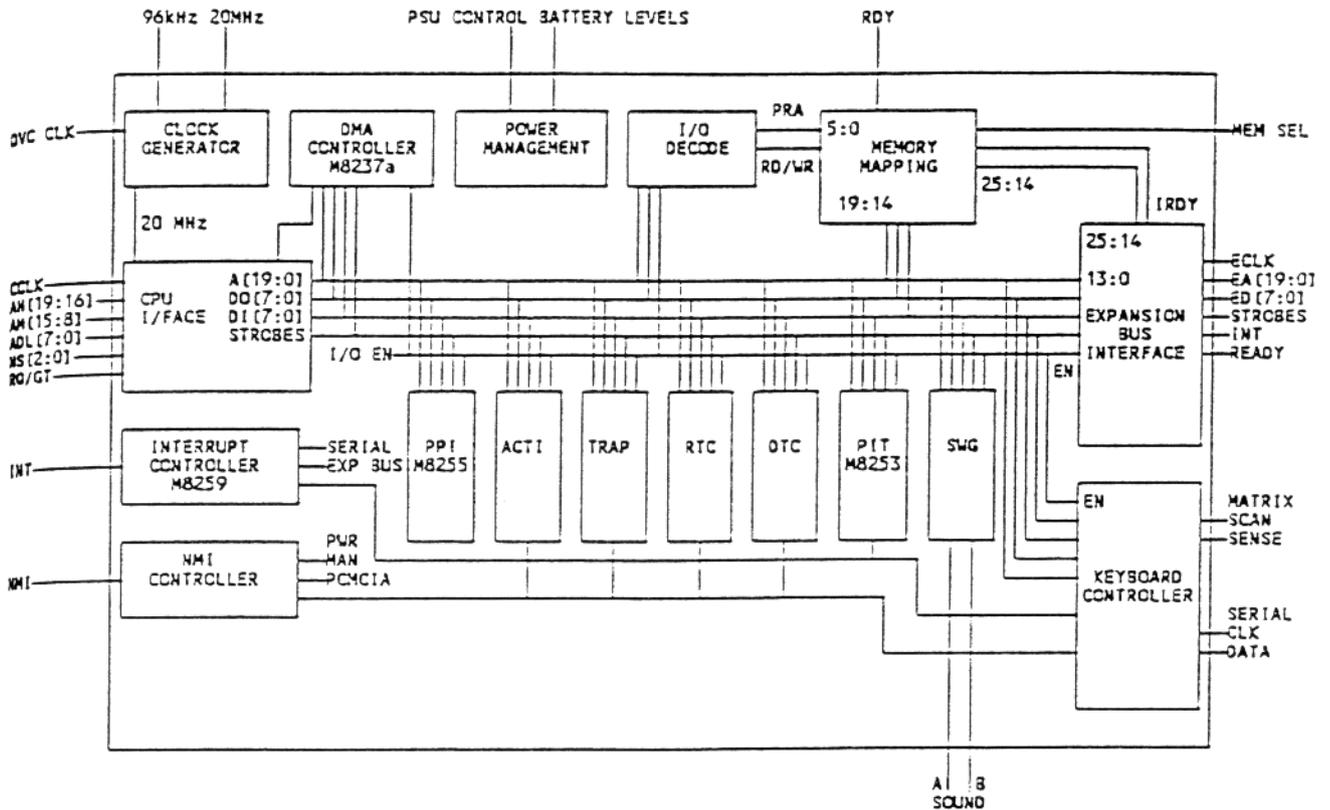
The processor is the MSM80C38A. For a data sheet, contact the OKI Electric Co.

11.2 The SPC ASIC

The SPC ASIC is a custom device which contains much of the circuits of the PC-3000, including:

- * M8237A direct memory access controller (DMAC)
- * M8259A interrupt controller (PIC)
- * NMI controller
- * M8253 programmable interval timer (PIT)
- * M8255 programmable peripheral interface (PPI)
- * Memory mapping
- * Address trapping
- * Activity detection
- * Sound generator
- * Keyboard interface
- * Real time clock (RTC) and tick timer
- * Status panel controller
- * Clock generator
- * Expansion bus interface

11.2.1 Block Diagram



11.2.2 SPC ASIC Pinouts

Pin	Signal	Description
1	NCE	Memory map mode select for DVC (output)
2	DCLK	DVC ASIC clock, 10MHz (output)
3	SPTI	Serial port interrupt (input)
4	PPTI	Parallel port interrupt (input)
5	NPSR3	PSRAM 3 select (output)
6	NPSR2	PSRAM 2 select (output)
7	NPSR1	PSRAM 1 select (output)
8	NPSR0	PSRAM 0 select (output)
9	NROM1	ROM 1 select (output)
10	NROM0	ROM 0 select (output)
11	NOTP1	OTPRAM 1 select (output)
12	VCC	Power supply
13	NOTP0	OTPRAM 0 select (output)
14	NJCR	PCMCIA register select (output)
15	NJEDB	PCMCIA interface enable (output)
16	NJEDA	PCMCIA interface enable (output)
17	GND	Ground
18	NLCE	PSRAM output enable (output)
19	NLWE	PSRAM write enable (output)
20	NCPUPE	CPU power enable (output)
21	NPSRPE	PSRAM power enable (output)
22	NLCOPE	LCD power enable (output)
23	NAMPPE	Sound output amplifier power enable (output)
24	NEXPPE	Expansion power enable (output)
25	NJCAPE	Memory card A power enable (output)
26	NJC3PE	Memory card A power enable (output)
27	NVPPPE	VPP power enable (for Flash memory) (output)
28	MCSA	Memory card A eject switch (input)
29	MCSB	Memory card B eject switch (input)

30	NHWRES	Reset switch (input)
31	EXSW	Expansion unit switch (input)
32	NTESTO	Test point
33	VCC	Power supply
34	SC32	Sound channel 1 (output)
35	SC31	"
36	SC30	"
37	SCA2	Sound channel 0 (output)
38	SCA1	"
39	GND	Ground
40	SCA0	Sound channel 0 (output)
41	MUX2	Multiplexed system information select (output)
42	MUX1	"
43	MUX0	"
44	ASI	Multiplexed system information (input)
45	DS1	"
46	SPD4	Scroll lock indicator (output)
47	SPD3	Num lock indicator (output)
48	SPD2	Caps lock indicator (output)
49	SPD1	Card 3 access indicator (output)
50	SPD0	Card A access indicator (output)
51	SPCK	LCD backplane clock, 64 Hz (output)
52	ERDY	CPU wait from DV/expansion bus (input)
53	RSET	Expansion bus reset (output)
54	NICC	Input indicating parity error from expansion bus
55	ECLK	Expansion bus clock, 5MHz (output)
56	VCC	Power supply
57	IRQ7	Interrupt (input)
58	IRQ6	Interrupt (input)
59	IRQ5	Interrupt (input)
60	IRQ4	Interrupt (input)
61	GND	Ground
62	IRQ3	Interrupt (input)
63	IRQ2	Interrupt (input)
64	NPSPD	PSRAM power down (input)
65	not used	
66	TC	Indicates last cycle of DMA sequence (output)
67	DACK0	DMA acknowledge (output)
68	DACK1	DMA acknowledge (output)
69	DREQ1	DMA request (input)
70	DACK2	DMA acknowledge (output)
71	DREQ2	DMA request (input)
72	DACK3	DMA acknowledge (output)
73	DREQ3	DMA request (input)
74	AEN	DMA cycle in progress (output)
75	ED0	System bus data line
76	ED1	"
77	VCC	Power supply
78	ED2	System bus data line
79	ED3	"
80	ED4	"
81	ED5	"
82	ED6	"
83	GND	Ground
84	ED7	System bus data line
85	NIW	I/O write strobe (output)
86	NIR	I/O read strobe (output)
87	GND	Ground
88	X20	96kHz crystal (input)
89	X21	"
90	VCC	Power supply
91	NMW	Memory write strobe (output)
92	NMR	Memory read strobe (output)
93	ALE	Address lines valid (output)
94	EA19	System bus address line
95	EA18	"
96	EA17	"
97	EA16	"
98	EA15	"
99	EA14	"
100	VCC	Power supply
101	EA13	System bus address line
102	EA12	"
103	EA11	"
104	EA10	"
105	GND	Ground
106	EA9	System bus address line
107	EA8	"
108	EA7	"
109	EA6	"

110	EAS	"
111	EA4	"
112	EA3	"
113	EA2	"
114	EA1	"
115	EA0	"
116	Not used	
117	Not used	
118	K19	Keyboard sense line (input)
119	K18	"
120	K17	"
121	VCC	Power supply
122	K16	Keyboard sense line (input)
123	K15	"
124	K14	"
125	K13	"
126	K12	"
127	GND	Ground
128	K11	Keyboard sense line (input)
129	X10	"
130	KS9	Keyboard scan line (output)
131	GND	Ground
132	X10	20MHz crystal
133	X11	"
134	VCC	Power supply
135	KS8	Keyboard scan line (output)
136	KS7	"
137	KS6	"
138	KS5	"
139	KS4	"
140	KS3	"
141	KS2	"
142	KS1	"
143	KS0	"
144	VCC	Power supply
145	CA19	CPU address line
146	CA18	"
147	CA17	"
148	CA16	"
149	GND	Ground
150	CA15	CPU address line
151	CA14	"
152	CA13	"
153	CA12	"
154	CA11	"
155	CA10	"
156	CA9	"
157	CA8	"
158	CA07	CPU address/data line
159	CA06	"
160	CA05	"
161	CA04	"
162	CA03	"
163	CA02	"
164	CA01	"
165	VCC	Power supply
166	CA00	CPU address/data line
167	NS2	CPU status (input)
168	NS1	CPU status (input)
169	NS0	CPU status (input)
170	NRQGT	RQ/GT bus request/grant input/output
171	GND	Ground
172	CRST	CPU reset (output)
173	INT	Interrupt (output)
174	NMI	NMI Interrupt (output)
175	CLK	CPU clock, 10MHz (output)
176	CRDY	CPU ready (output)

11.2.3 The SPC ASIC Control Registers

The following registers can be used to control the SPC ASIC, but only after writing 44H to the SPC key register, I/O address 8400H. Writing any other value to this register locks the SPC I/O control.

Address	Register	Comment
8400	Key register	00H read back if locked, 01H if unlocked
8401	LIMIO	Memory map I/O base
8402	ENABLE	See DVC ASIC description
8403	SRPS	"
8404	LIND	"
8405	LDAT	"
8406	PCNTR	Power control register
8407	CCNTR	Clock control register
8408	CPCG	CPU clock speed
8409	RCMP	PCMCIA programming control
840A	PASR	MB255 status latch
840B	PASR	"
840C	NMI08	SPC NMI vectors
840D	NMI09	"
840E	NMI0A	"
840F	NMI0B	"
8410	SISR	SPC interrupt source register
8411	SISE	SPC interrupt enable
8412	PSIR	Power supply int. register
8413	PSIE	Power supply int. enable
8414	PSIS	Power supply status
8415	ISIR	Internal service int. register
8416	ISIE	Internal service int. enable
8417	MIR	Memory int. register
8418	MIE	Memory int. enable
8419	MIS	Memory status
841A	RSTR	CPU reset source register
841B	KSTR	LCD status register
841C..F	**	**
8420	ATRO	Address trap
8421	ATR1	"
8422	ATR2	"
8423	**	**
8424	MAVO	Memory access violation
8425	MAV1	"
8426	MAV2	"
8427	**	**
8428	ACR lsb	Activity count register
8429	ACR	"
842A	ACR msb	"
842B	ACM	Activity mask register
842C	SWG0	Sound channel 0
842D	SWG0	"
842E	SWG1	Sound channel 1
842F	SWG1	"
8430	SCR-ISCR	Scan code for last key
8431	ARR	Keyboard auto repeat count
8432	PDR lsb	Keyboard power down
8433	PDR msb	"
8434	WSRO	Keyboard warm start scan code
8435	WSR1	"
8436	WSR2	"
8437	SKWR	Single key wake-up scan code
8438..F	**	**
8440	TCR lsb	DTC tick count register
8441	TCR	"
8442	TCR	"
8443	TCR msb	"
8444	TKI lsb	DTC tick interrupt register
8445	TKI	"
8446	TKI	"
8447	TKI msb	"
8448	TMI lsb	DTC timer interrupt register
8449	TMI	"
844A	TMI	"
844B	TMI msb	"
844C..F	**	**
8450	RTR lsb	RTC counter register
8451	RTR	"
8452	RTR	"
8453	RTR	"
8454	RTR msb	"
8455..7	**	**
8458	RTI lsb	RTC interrupt register
8459	RTI	"
845A	RTI	"
845B	RTI	"
845C	RTI msb	"
845D	TR	DTC timer control register
845E..F	**	**

11.2.4 LIM EMS

The EMM.SYS installable device driver provides expanded memory management which complies with LOTUS/INTEL/MICROSOFT Expanded Memory Specification 4.0 (LIM 4.0), with the following limitations:

- 1 Memory mapping is in 16KByte pages only, so raw pages are not supported. (Affects functions 26 and 27.)
- 2 Non-volatile pages are not supported. (Affects functions 19 and 29.)
- 3 Hardware alternate register sets are not supported. (Affects function 28.)
- 4 The EMM allows one context save per handle. (Affects functions 8 and 9.)
- 5 DMA register sets are not supported. (Affects function 28.)

11.2.5 Memory Mapping And Access Violations

The PC-3000 physical memory is 1MByte, divided into 64 16KByte pages. For each page a mapping register selects the physical device to address in that range and how it can be accessed (read-only or read-write). CPU and DMA cycles are both mapped using the same mechanism.

The memory map registers are as follows:

Register	Address	Comments
0	00000..03FFF	
1	04000..07FFF	
2	08000..0BFFF	
3	0C000..0FFFF	
4	10000..13FFF	
5	14000..17FFF	
6	18000..1BFFF	
7	1C000..1FFFF	
8	20000..23FFF	
9	24000..27FFF	
10	28000..2BFFF	
11	2C000..2FFFF	
12	30000..33FFF	
13	34000..37FFF	
14	38000..3BFFF	
15	3C000..3FFFF	256KByte boundary
16	40000..43FFF	
17	44000..47FFF	
18	48000..4BFFF	
19	4C000..4FFFF	
20	50000..53FFF	
21	54000..57FFF	
22	58000..5BFFF	
23	5C000..5FFFF	
24	60000..63FFF	
25	64000..67FFF	
26	68000..6BFFF	
27	6C000..6FFFF	
28	70000..73FFF	
29	74000..77FFF	
30	78000..7BFFF	
31	7C000..7FFFF	512KByte boundary
32	80000..83FFF	
33	84000..87FFF	
34	88000..8BFFF	
35	8C000..8FFFF	
36	90000..93FFF	
37	94000..97FFF	
38	98000..9BFFF	
39	9C000..9FFFF	640KByte boundary

40	A0000..A3FFF	
41	A4000..A7FFF	
42	A8000..ABFFF	
43	AC000..AFFFF	
44	B0000..B3FFF	Used by MOA
45	B4000..B7FFF	Used by MOA
46	B8000..BBFFF	Used by CGA
47	BC000..BFFFF	Used by CGA
48	C0000..C3FFF	
49	C4000..C7FFF	
50	C8000..CBFFF	
51	CC000..CFFFF	
52	D0000..D3FFF	
53	D4000..D7FFF	
54	D8000..DBFFF	
55	DC000..DFFFF	
56	E0000..E3FFF	
57	E4000..E7FFF	
58	E8000..EBFFF	
59	EC000..EFFFF	
60	F0000..F3FFF	Used by BIOS and XBIOS
61	F4000..F7FFF	"
62	F8000..FBFFF	"
63	FC000..FFFFF	"

To access a register, use I/O to the following addresses:

Address	Register	Description
BASE+0	PRN5..0	Page register select [1]
BASE+1	PRN5..0	Page register select [1]
BASE+2	M7..0	Page register LSB
BASE+3	M15..3	Page register MSB

Notes:

* BASE is defined by the SPC configuration register LIMIO.

[1] Both addresses map to the same register.

Each register is 16 bits wide (M15..0). Bits 15..12 select the device to map to that address range:

MA15..12	Device	Comment
0	OTPRM0	
1	Not used	
2	ROM0	
3	Not used	
4	PSRAM0	
5	PSRAM1	
6	PSRAM2	Optional device
7	PSRAM3	Optional device
8	PCMCIA A R/W	Read/write access
9	PCMCIA A R	Read access only
A	PCMCIA B R/W	Read/write access
B	PCMCIA B R	Read access only
C	SRAM R/W	Read/write access
D	SRAM R	Read access only
E	Expansion bus	
F		No memory device selected

Bits 11..0 of the memory map register select the page and control read-only access:

1 For read-only devices (OTPRM0 and ROM0) and PCMCIA cards, MA11..0 allows selection of any 16KByte page in a 64 MByte range. If the device has less than 64 MByte, the address wraps.

52 2 For PSRAM, MA7..0 allows selection of any 16KByte page in a 4096KByte range. MA11..8 controls access to 4KByte segments within

the page:

bit	If 0	If 1
MA8	Segment 0 is R/W	Segment 0 is read-only
MA9	Segment 1 is R/W	Segment 1 is read-only
MA10	Segment 2 is R/W	Segment 2 is read-only
MA11	Segment 3 is R/W	Segment 3 is read-only

If a write is attempted to a read-only segment, a memory access violation (MAV) is generated and the write fails.

- 3 For SRAM, MA3..0 allows selection of any 16KByte page in a range of 256KByte. For device select D (SRAM R) MA11..4 is ignored. For device select C (SRAM R/W), MA11..4 controls access to 2KByte segments with the page:

bit	If 0	If 1
MA4	Segment 0 is R/W	Segment 0 is read-only
MA5	Segment 1 is R/W	Segment 1 is read-only
MA6	Segment 2 is R/W	Segment 2 is read-only
MA7	Segment 3 is R/W	Segment 3 is read-only
MA8	Segment 4 is R/W	Segment 4 is read-only
MA9	Segment 5 is R/W	Segment 5 is read-only
MA10	Segment 6 is R/W	Segment 6 is read-only
MA11	Segment 7 is R/W	Segment 7 is read-only

If a write is attempted to a read-only segment, a memory access violation (MAV) is generated and the write fails.

- 4 For the expansion bus, MA5..0 allows access to any 16KByte page within a 1MByte range. MA11..6 is ignored.

Memory access violations will occur when attempting to:

- * Write to a read-only RAM page.
- * Write to a ROM or OTPROM.
- * Write to a write-protected PCMCIA card.
- * Read or write a PCMCIA card which is not present.

The access will fail and cause a MAVI NMI, latching the CPU address and cycle type. These can be read from the following SPC ASIC registers:

Status	Register	Description
A7..0	MAV0	CPU/DMA address
A15..8	MAV1	CPU/DMA address
A19..16	MAV2 03..0	CPU/DMA address
R/W	MAV2 04	Access type: 0=read, 1=write
D/C	MAV2 05	Cycle type: 0=data, 1=code
DMA/CPU	MAV 06	Device: 0=DMA, 1=CPU

Note that the MAVI interrupt is cleared by reading MAV2.

11.2.6 Address Trapping

Address trapping allows the PC-3000 to intercept attempts to read or write from specified memory locations. The trap address and access type is set by SPC ASIC registers ATR0..2:

Register	Description
ATR0	Trap address, A7..0
ATR1	Trap address, A15..8
ATR2	03=0: trap address, A19..16 04=1: enable CODE trap 05=1: enable NRD trap 06=1: enable NWR trap 07: ignored.

To trap a code read, enable both CODE and NRD.

When a memory access is trapped, the PATR interrupt is generated. If the cycle type is a code read, the interrupt is delayed by four code read cycles (the length of the instruction pre-fetch queue). The PATR interrupt is cleared by reading ATR2.

11.2.7 8237A DMA Controller (DMAC)

The DMAC is described in chapter 9.

11.2.8 Reset

There are three types of reset on the PC-3000: the SPC ASIC hardware reset, keyboard warm start reset and an interrupt while the CPU is powered down.

Operation of the reset switch produces the NHWRES and DRSET signals. NHWRES resets the SPC ASIC and DRSET the DVC ASIC.

The reset source can be read from the RSTR register (841AH). RSTR is read-only and is cleared when read:

Bit	Signal	Reset source
07=1	HRST	Hardware reset
06=1	KRST	Keyboard warm start reset
05=1	SRST	Interrupt reset

11.2.9 8259 Programmable Interrupt Controller (PIC)

The PIC is described in chapter 9.

11.2.10 8253 Programmable Interval Timer (PIT)

The M8253 PIT provides three programmable timer/counters, used as follows:

Counter 0: General purpose
Counter 1: Refresh timer (DMA channel 0)
Counter 2: Tone generator

GATE 0,1: Tied ON
 GATE 2: Controlled by M8255 PBO
 OUT0: IRQ0
 OUT1: Refresh request, DMA channel 0
 OUT2: Speaker tone, logically ANDed with M8255 PB1.

The clock frequency is 1.1932 MHz (+/- 0.1%), derived from the 20 MHz clock by the divide sequence 8,8,9,8,8,9,8,9... The clock can be enabled and disabled by bit 5 of the CCNTR register.

11.2.11 8255 Programmable Peripheral Interface (PPI)

The ASIC emulates a M8255 PPI, permanently programmed as follows:

Port A: Mode 0, input
 Port B: Mode 0, output
 Port C: Mode 0, input

The ports are used as follows:

Port A:

Bit	Input if PB7=0	Input if If PB7=1
07	KBD7	PASR7 (number of FDCs, MSB)
06	KBD6	PASR6
05	KBD5	PASR5
04	KBD4	PASR4
03	KBD3	PASR3
02	KBD2	PASR2
01	KBD1	PASR1
00	KBD0	PASR0

KBD0..7 are read from the keyboard register. PASR0..7 are read from the system configuration register.

Port B:

Bit	Signal	Output
07	PB7	Enable PASR0..7/KBD0..7 on port A (see above)
06	PB6	Enable incoming keyboard clock
05	PB5	Prevent I/O check from causing NMI
04	PB4	No effect
03	PB3	No effect
02	PB2	Enable PASR8..B/PASRC..F on port C 00..3 (see below)
01	PB1	Loudspeaker drive
00	PB0	M8253 gate 2 (modulate speaker sound)

Setting PB7 enables PASR0..7 on port A, clears the keyboard data path and clears and disables the keyboard interrupt. Resetting PB7 enables the keyboard data path and interrupts.

Resetting PB6 forces the keyboard clock low to reset the keyboard.

Port C:

Bit	Input	
07	Always 0	
06	External parity error (I/O check)	
05	M8253 OUT2	
04	Always 0	
03	If PB2=0	If PB2=1
02	PASRF	PASRB
01	PASRE	PASRA
00	PASRD	PASR9
	PASRC	PASR8

PASRF..D are not used. PASRC..C defines the amount of RAM fitted, as follows:

C	B	A	9	8	RAM
0	1	1	1	0	512KByte
0	1	1	1	1	544KByte
1	0	0	0	0	576KByte
1	0	0	0	1	608KByte
1	0	0	1	0	640KByte

11.2.12 Keyboard Interface

The keyboard interface produces scan codes based on a 10 x 10 key switch matrix, in the range 0..78H. It also sets a flag to indicate whether the key was pressed or released.

The keyboard controller scans each switch in the keyboard matrix in turn. It does this by forcing each of KS0..9 (scan outputs) high in turn and then testing each of KI0..9 (sense inputs). The scanning frequency is set by the KCLK clock.

The controller keeps a record of the previous state of each switch, so it can determine if a key has been pressed or released. If a change occurs, it places a number representing the switch position within the matrix in the scan-code register (SCR), along with the press/release flag and then issues the keyboard interrupt (KINT).

The BIOS KINT service routine reads the scan code from the SCR and converts it to an IBM-compatible scan code which is stored in the ISCR register. This generates an Int 9H via IRQ1.

If a key is held down, the controller will issue further interrupts at intervals dictated by the auto-repeat register (ARR), to implement autorepeat. ARR stores the number of scans until auto-repeat starts. Once autorepeat starts it issues one interrupt per scan.

The warm start facility stores a combination of three scan codes in the warm start registers (WSRs), for CTRL, ALT and DEL. If these three keys are all held down during a scan, a warm start reset is generated for one KCLK cycle, which will reset the CPU and set the KRST bit in the reset source register (RSTR). This provides an additional way of rebooting a program which has hung, that is not provided on an IBM XT.

The single key wake-up register (SKWR) holds a scan code in D6..0. When this key is found, a wake-up interrupt (WINT) is generated for one KCLK cycle.

11.2.13 Timer

The SPC ASIC timer provides a 32 bit counter (TCR) with two associated interrupts (TKI and TMI), and a 40 bit counter (RTR) used as an RTC with an associated interrupt (RTI). Operation is controlled by an 8 bit register (TR).

The 32 bit counters are incremented by the tick clock TCLK (18.28 Hz x 1), while the RTC is incremented by the RTC clock (128 Hz x 3).

The registers are as follows:

Name	Bits	Description	
TCR	32	Tick counter register. R/W. Increments each cycle of TCLK, on the rising edge of the waveform.	
TKI	32	Tick interrupt register. R/W. Sets the level of the TCR at which the TICI interrupt occurs. Used for tick interrupts.	
TMI	32	Timer interrupt register. R/W. Sets the level of the TCR at which the TMI interrupt occurs. Used for timing loops.	
RTR	40	RTC counter register. R/W. Increments each cycle of RCLK, on the rising edge of the waveform. Used for the time and date.	
RTI	40	RTC interrupt register. R/W. Sets the level of the RTR at which the RTCI interrupt occurs. Used for the alarm function.	
TR	8	Timer control register. Controls operation of the timer as follows:	
	Bit	Signal	Access allowed
	7	not used	R
	6	RTS	R
	5	TTS	R
	4	FRTC	R/W
	3	FTC	R/W
	2	ETMI	R/W
	1	ETCI	R/W
	0	ERTI	R/W

ETMI controls the timer interrupt: 1 enables, while 0 clears and disables any pending interrupt.

ETCI controls the tick interrupt: 1 enables, while 0 clears and disables any pending interrupt.

ERTI controls the RTC interrupt: 1 enables, while 0 clears and disables any pending interrupt.

FTC controls the tick count: 1 freezes incrementing of the TCR so it can be read. Re-enable (by setting to 0) within 14 mSec to avoid missing a tick.

FRTC controls the RTC count: 1 freezes incrementing of the RTR so it can be read. Re-enable (by setting to 0) within 2 mSec to avoid missing a clock.

TTS is the ticker timer status: 1 means that the tick counter has been loaded as a result of writing to the msb of the TCR, 0 means that it has not been written.

RTS is the RTC status: 1 means that the RTC counter has been loaded as a result of writing to the msb of the RTR, 0 means that it has not been written.

After a hardware reset, TTS and RTS will be 0 until their counters have been loaded and then will remain set to 1.

11.2.14 LCD Status

The LCD status panel has five segments which are used to display the Num Lock, Caps Lock, Scroll Lock, Drive A and Drive B status. These are driven by five independent outputs (SPD4..0), in phase with the 64 Hz LCD backplane clock (SPCK).

The outputs are controlled by writing to the KSTR register:

Bit	Use	Comment
-----	-----	---------

07	Enable	0 if all other signals low.
06		Not used.
05		Not used.
04	SP04	Segment 4 drive.
03	SP03	Segment 3 drive.
02	SP02	Segment 2 drive.
01	SP01	Segment 1 drive.
00	SP00	Segment 0 drive.

11.2.15 Clock Generation

The PC-3000 has two crystal oscillators, 96 kHz and 20 MHz, from which all clocks are derived, as follows.

The clocks derived from 20 MHz are controlled by the CCNTR register:

Bit	If set, enables
07	CPU/DMA clock
06	DVC clock
05	PIT clock
04..0	Not used

When a clock is stopped, it will always stop in its low state. If all three clocks are stopped, the 20 MHz oscillator stops too.

The CPU clock is 10 MHz, with a programmable delay between cycles of between 0 and 31 clock cycles (0 to 3.1 microseconds), producing an effective clock speed of between 10 MHz and 1 MHz. It is stopped by clearing CCNTR D7 or PCNTR D7 (which powers down the CPU). It can be restarted by an interrupt.

The DMA clock is 5 MHz and is controlled by CCNTR D6.

The expansion bus clock is 5 MHz and is only generated if an expansion unit is fitted and powered up.

The PIT clock is notionally 1.1932 MHz, but is derived by using the division sequence 8,8,9,8,8,9,8,9... to give an actual clock of 1.194 MHz.

The 96 kHz oscillator never stops (unless all power is lost). It is used to generate the tick clock (TCLK), RTC clock (RCLK), keyboard clock (KCLK), etc.

11.3 The DVC ASIC

The DVC ASIC is a custom device which provides PC-compatible MDA, CGA and AT&T video controllers, a 8250B based serial port and Centronics-compatible printer port. (The AT&T video mode is not used in the PC-3000 design.)

The ASIC can interface to the system two different ways:

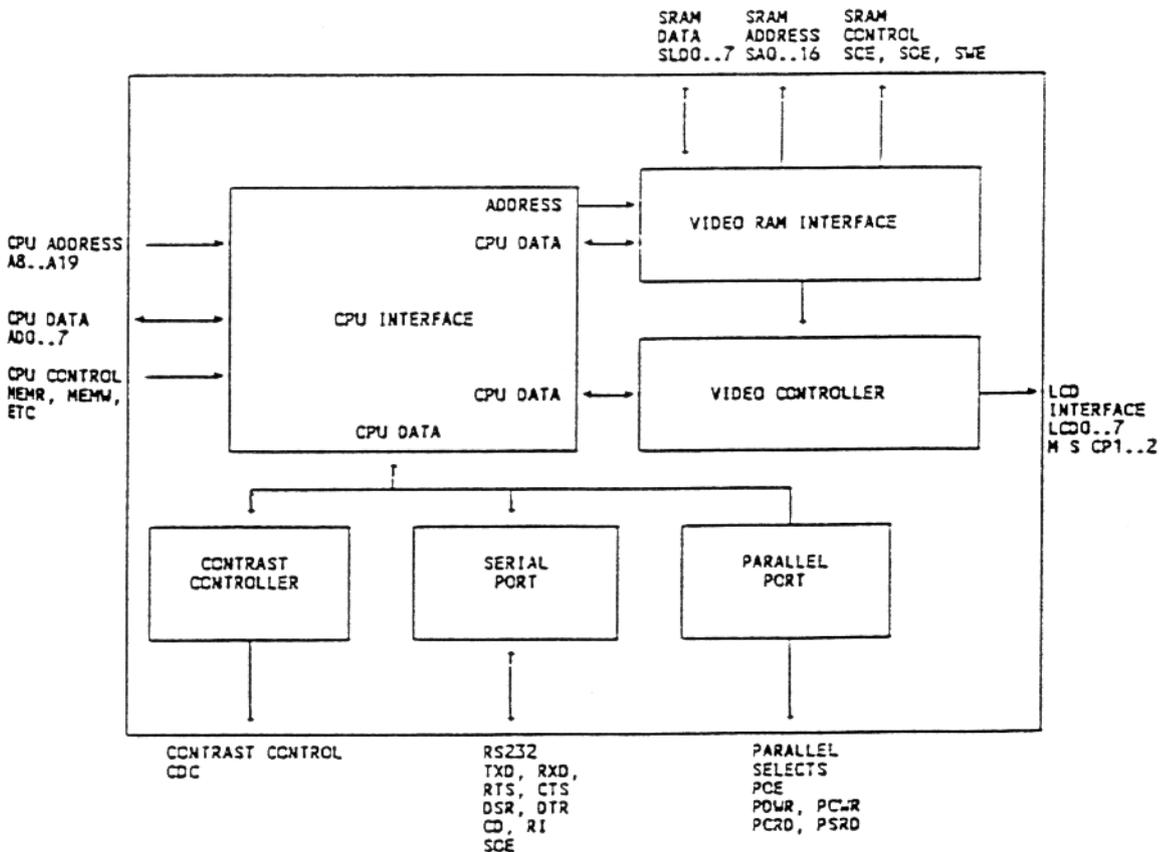
- * 8088 CPU max mode
- * 8088 CPU max mode with memory mapping

CPU max mode is selected when NCE is low and CPU max mode with memory mapping when NCE is high. NCE is controlled by the SPC ASIC.

The mode affects the interface signals as follows:

Pin	8088 max	Memory mapped
A19..14	A19..14	MA19..14
NCE	0V	NCE
NS0	NS0	NRD/NS0
NS1	NS1	NWR/NS1
NS2	NS2	ICM/NS2
ALE	0V	ALE/0V

11.3.1 Block Diagram



11.3.2 Pinouts

pin	Signal	Description
1	GND	Ground
2	VCC	Power supply
3	SA15	SRAM address line
4	SRWE	SRAM write enable (output)
5	SA13	SRAM address line
6	SA8	"
7	SA9	"
8	SA11	"
9	SROE	SRAM output enable (output)
10	SA10	SRAM address line
11	SRCE	SRAM chip enable (output)
12	SLD7	SRAM/LCD data line
13	SLD6	"
14	SLD5	"
15	SLD4	"
16	SLD3	"
17	SA16	SRAM address line
18	SA14	"
19	SA12	"
20	SA7	"
21	SA6	"
22	SA5	"
23	SA4	"
24	SA3	"
25	SA2	"
26	SA1	"
27	SA0	"
28	GND	Ground
29	VCC	Power supply
30	SLD0	SRAM/LCD data line
31	SLD1	"
32	SLD2	"
33	CP1	LCD line clock pulse (output)
34	CP2	LCD pixel clock (output)
35	LF	LCD line sync (output)
36	DF	LCD frame toggle (output)
37	LCD0	LCD data line (output)
38	LCD1	"
39	LCD2	"
40	GND	Ground
41	LCD3	LCD data line (output)
42	LCD4	"
43	LCD5	"
44	LCD6	"
45	LCD7	"
46	CDC	Contrast controller voltage (output)
47	PDWR	Printer data write strobe (output)
48	PCWR	Printer control write strobe (output)
49	PCRD	Printer control read strobe (output)
50	PSRD	Printer status read strobe (output)
51	PCE	Printer buffer output enable (output)
52	VCC	Power supply
53	GND	Ground
54	CLK	LCD clock (input)
55	MACX	Printer ACK (input)
56	PINT	Printer interface interrupt (output)
57	A19	CPU address line
58	A18	"
59	A17	"
60	A16	"
61	A15	"
62	A14	"
63	A13	"
64	A12	"
65	A11	"
66	A10	"
67	A9	"
68	A8	"
69	AD7	CPU address/data line
70	AD6	"
71	AD5	"
72	AD4	"
73	AD3	"
74	AD2	"
75	AD1	"
76	AD0	"
77	S0	CPU status (input)
78	S1	CPU status (input)
79	VCC	Power supply

80	GND	Ground
81	SZ	CPU status (input)
82	READY	CPU wait (output)
83	RST	DVC reset (input)
84	NCE	Memory map control (input)
85	ALE	Address lines valid (not used)
86	HLDA	DMA cycle in progress (input)
87	AOEN	Not used
88	DCEN	Not used
89	DDIR	Not used
90	ISA	ISA/CPU bus enable (CPU bus)
91	TXD	RS232 Data Out (output)
92	RXD	RS232 Data In (input)
93	RTS	RS232 Request To Send (output)
94	CTS	RS232 Clear To Send (input)
95	DSR	RS232 Data Set Ready (input)
96	DCD	RS232 Data Carrier Detect (input)
97	DTR	RS232 Data Terminal Ready (output)
98	RI	RS232 Ring In (input)
99	SINT	RS232 interrupt (output)
100	SEN	RS232 power enable (output)

11.3.3 The DVC ASIC Control Registers

The following registers can be used to control the DVC ASIC, after writing 44H to the SPC key register, I/O address 8400H. Writing any other value to this register locks the SPC I/O control.

Address	Register	Description
8401	LIMIO	(SPC ASIC register)
8402	ENABLE	I/O configure
8403	SRPS	SRAM page select
8404	LIND	LCD index register
8405	LDAT	LCD data
8406	PMEN	Power control register

D5..D0 of the ENABLE register controls the DVC configuration, as follows. D6 and D7 are not implemented.

D1..D0 control the parallel port:

D1	D0	Effect
0	0	PPI disabled (low power mode)
0	1	PPI enabled at primary address (378H..37FH)
1	0	PPI enabled at secondary address (278H..27FH)
1	1	PPI enabled at MDA address (38CH..3BFH)

D3..D2 control the serial port:

D3	D2	Effect
0	0	M8250B disabled (CLK off)
0	1	M8250B enabled at primary address (3F8H..3FFH)
1	0	M8250B enabled at secondary address (2F8H..2FFH)
1	1	M8250B disabled (CLK off)

D5..D4 control the video controllers:

D5	D4	Effect
0	0	All video controllers disabled (CLK off)
0	1	MDA enabled
1	0	CGA enabled
1	1	AT&T enabled (not used)

D6..D0 of the SRPS register allows access to the entire 128KByte SRAM, selecting which 1KByte boundary of the device to map the CPU address map to. In MDA mode the SRPS works relative to the base of the SRAM; in CGA mode, it works relative to 8000H in the SRAM.

D7 of SRPS controls memory wrapping in MDA and CGA modes. If set, 32KByte of DVC memory is directly accessible without paging, starting at the base address for the video mode.

The LIND register is used to select the LCD configuration register to access at LDAT. For details, see "LCD Video Controller" (section 11.3.9).

The PMEN register shadows bits 3, 1 and 0 of the PCNTR register in the SPC ASIC, which controls power management. For details, see the description of the PCNTR register in "The SPC ASIC Control Registers", section 11.2.3.

11.3.4 D6845 Video Controller

The D6845 video controller emulates the standard 6845 video controller with modifications to suit use with an LCD rather than a conventional monitor. To avoid problems when changing screen modes, use the BIOS functions, rather than direct access to the hardware.

The registers are as follows:

Register	Name	Comment
R0	Horizontal total	Not implemented
R1	Horizontal display	MDA = 80 [1] CGA alpha 40*25 = 40 CGA alpha 80*25 = 80 CGA graphics = 40
R2	H sync position	Not implemented
R3	H+V sync width	Not implemented
R4	Vertical total	Not implemented
R5	Vertical total adj	Not implemented
R6	Vertical displayed	MDA = 25 [1] CGA alpha = 25 CGA graphics = 100
R7	V sync position	Not implemented
R8	Interlace + skew	Not implemented
R9	Maximum raster	Locked MDA fixed = 7 [2] CGA text = 7 CGA graphics 2 = 1 CGA graphics 1 = 1
R10	Cursor start	[3]
R11	Cursor end	[3]
R12	Start address	[4]
R13	Start address	[4]
R14	Cursor address	
R15	Cursor address	

R16	Light pen	Provided, although light pen connection is not supported.
R17	Light pen	" "

Notes:

- [1] These registers are not programmable in MDA mode.

These registers can be locked in MDA mode by setting bit 4 of MCR1 in the LCD controller. This forces the maximum character raster to 7 and modifies the cursor start raster (R10) so that any cursor start raster between 8 and 14 will be displayed on the last scan line (7). A value of more than 14 will make the cursor invisible.

- [2] These registers are not programmable. The value used depends on the mode.
- [3] Cursor control bits (D5 and D6) only are programmable.
- [4] In MDA modes, display start is relative to the base of the SRAM. In other modes, display start is at an offset of 8000H into the SRAM.

11.3.5 Colour mapping

The LCD provides 4 gray levels, produced by turning pixels on and off during an 8 frame cycle:

GS0 always off
 GS1 DSGS1 D0..7 define the ON frames
 GS2 DSGS2 D0..7 define the ON frames
 GS3 always on

DSGS1 and DSGS2 are LCD control registers (see "LCD Video Controller", section 11.3.9), where each bit signifies that the pixel should be on for that frame. Logical colours are mapped to gray scales to display as follows:

In MDA modes:

- * GS0 is used for normal white on black, background and inverse black on white, foreground.
- * GS1 is used for normal white on black, foreground and inverse black on white, background.
- * GS2 is not used.
- * GS3 is used for normal white on black highlighted, foreground and inverse black on white highlighted, background.

In CGA alpha modes:

- * GS0 is used for black background or foreground
- * GS1 is used for a coloured background, or the foreground on a black background
- * GS2 is used for the foreground on a coloured background
- * GS3 is used for intensified foreground on a coloured background

In graphics mode 1 (300*200):

- * GS0 is used for bit 1=0, bit 0=0 and background.
- * GS1 is used for bit 1=0, bit 0=1, or background if = colour.
- * GS2 is used for bit 1=1, bit 0=0, of background if = colour.
- * GS3 is used for bit 1=1, bit 0=1, of background if = colour.

In graphics mode 2 (640*200):

- * GS0 is used for background and foreground if black.
- * GS3 is used for foreground.

11.3.6 MDA Video Controller

The MDA implementation is standard, except that the Character matrix is 8x8, not 9x14.

11.3.7 CGA Video Controller

The CGA implementation is standard.

11.3.9 LCD Video Controller

The LCD controller can be used with other sizes of LCD by using the LCD configuration registers. To access a register, write the index number to 8404H, then access the register at 8405H. The index numbers are:

Index	Register	Comment
0	OTH	Horizontal display + border in characters.
1	OSH	Horizontal display size in characters.
2	MALT	Number of lines per LCD DF signal alternation.
3	TPVS	Vertical size.
4	DSTV	Vertical display + status in pixels.
5	DSV	Vertical display in pixels.
6	OSOL	LCD offset address lsb (in characters).
7	OSOU	" " msb " "
8	MCRO	Mode Control Register 0.
9	MCR1	Mode Control Register 1.
10	DSST	Display status start address/512.
11	DSCT	Character table start address/512.
12	DSGS1	Gray scale set GS1.
13	DSGS2	Gray scale set GS2.
14	DCC	Contrast voltage.

These registers are not relevant to normal operation of the PC-3000 and will not be described further.

11.3.10 Contrast Controller

The LCD contrast is controlled by the CDC output from the DVC ASIC, a 300 Hz signal with a mark:space ratio of between 0:128 and 128:128. Its duty cycle is set by the DCC register:

DCC	CDC	Contrast
0	low	low
1..7FH	300Hz	depends on DCC value
80..FFH	high	high

64 The CDC mark space ratio modulates VDD to producing a -VEE voltage to the LCD contrast circuits of between 0V (off) and -16V (max).

11.9 Expansion Bus

11.9.1 Expansion Bus Pinouts

The expansion bus pinouts are as follows:

Pin	Signal	Description
1	GND	Ground
2	PACIN	AC input from expansion bus
3	PACIN	AC input from expansion bus
4	n/c	
5	n/c	
6	n/c	
7	EXSW	Input. Expansion unit switch
8	EXPDET	Expansion unit detect (input)
9	GND	Ground
10	EA0	System bus address line. A valid address for all
11	EA1	memory cycles and I/O cycles to external devices.
12	EA2	"
13	EA3	"
14	EA4	"
15	EA5	"
16	EA6	"
17	EA7	"
18	EA8	"
19	EA9	"
20	EA10	"
21	EA11	"
22	EA12	"
23	EA13	"
24	EA14	"
25	EA15	"
26	EA16	"
27	EA17	"
28	EA18	"
29	EA19	"
30	AEN	Indicates a DMA cycle in progress.
31	ERDY	CPU READY: output by a device on the expansion bus to stretch cycles.
32	ED0	System bus data/address lines. (See note 1)
33	ED1	"
34	ED2	"
35	ED3	"
36	ED4	"
37	ED5	"
38	ED6	"
39	ED7	"
40	IOC*	Inout. Indicates a parity error from a device on the bus
41	GND	Ground
42	PACIN	AC input from expansion bus
43	PACIN	AC input from expansion bus
44	EXPPE*	Expansion bus power enable
45	EXPBV2	Expansion bus device battery low
46	EXPBV1	Expansion bus device battery flat
47	KBC	External keyboard (input)
48	KBD	External keyboard (input)
49	PACOUT	AC output to expansion bus
50	PACOUT	AC output to expansion bus
51	PACOUT	AC output to expansion bus
52	CPUPE*	Main power enable (output)
53	ALE	Indicates access to bus or memory card cycle. [2]
54	TC	Indicates the last DMA cycle of a DMA sequence.
55	DACK2	Output. DMA acknowledge
56	IRQ3	Inputs, used by devices on the bus to request
57	IRQ4	attention.
58	IRQ5	"
59	IRQ6	"
60	IRQ7	"
61	ECLK	A 5 MHz clock with a 50:50 duty cycle.
62	DACK0	Output. DMA acknowledge
63	DREQ1	Input. DMA request
64	DACK1	Output. DMA acknowledge
65	DREQ3	Input. DMA request
66	DACK3	Output. DMA acknowledge
67	IR*	I/O read strobe, active for expansion bus cycles
68	IW*	I/O write strobe, active for expansion bus cycles
69	MR*	Memory write strobe, active for expansion bus cycles

70	MW*	Memory read strobe, active for expansion bus cycles
71	TP1	Test point
72	TP2	"
73	TP3	"
74	TP4	"
75	DREQ2	Input. DMA request
76	GND	Ground
77	IRQ2	Used by a device on the bus to request attention.
78	CPUPE*	CPU power enable (output)
79	RESET	All devices on bus should reset to initial state.
80	GND	Ground
81	GND2	"
82	GND2	"

Notes:

- * Means that the signal is active low.
- [1] ED7..0 are data transfer lines which will also have a valid address (A25..20 on ED5..0) during ALE while accessing a memory card.
- [2] ALE indicates access to a memory card or an expansion bus cycle, this shows the address on EA19..0 is valid. Addresses are latched on the falling edge of ALE. ALE is low during refresh cycles.
- [3] The ISA bus signal OSC is not supported.
- [4] In this table, "output" means output by the PC-3000 to the expansion bus.

11.9.2 Timing

The expansion bus timing is based on the IBM PC expansion bus; refer to the IBM PC Technical Reference for guidelines. Note that the bus clock is 5 MHz, not 4.77 MHz.

Expansion bus memory cycles and memory refresh cycles normally take 4 clock cycles (800 nSec) to complete. Expansion bus I/O cycles and DMA cycles (other than refresh) normally take 5 clock cycles (1000 nSec) to complete.

However, slow devices can stretch memory, I/O, DMA and memory refresh cycles (in multiples of 200 nSec) by asserting -ERDY.

11.10 Memory Card Drives

Insertion of a PCMCIA memory card generates an NMI (MCDA/MCDB) which causes the CPU to turn the appropriate card buffer on. To remove the card a user must press a mechanical switch, which issues another NMI (MCSA/MCSB) that turns the buffer off. The card buffers also turn off when the PC-3000 is turned off.

5V power (VCC) is normally supplied to a memory card while it is inserted and the PC-3000 is turned on (but see section 7.10). Power is controlled by the JCAPE- and JCBPE- outputs from the SPC ASIC.

12V power (VPP) is only generated and supplied when writing to a FLASH memory card. It is controlled by the VPPPE- output from the SPC ASIC.

11.10.1 Card Connector Pinouts

The memory card connector is a 2 x 34 way connector with the following pinouts:

Pin	Signal	Description
1	GND	Ground
2	JD3	Data line
3	JD4	"
4	JD5	"
5	JD6	"
6	JD7	"
7	-JCE01	Card enable
8	JA10	Address line
9	-JCE	Output enable
10	JA11	Address line
11	JA9	"
12	JA8	"
13	JA13	"
14	JA14	"
15	-JWE	Write enable
16	not used	
17	JAVCC	Vcc
18	JAVPP	Vpp
19	JA16	Address line
20	JA15	Address line
21	JA12	"
22	JA7	"
23	JA6	"
24	JA5	"
25	JA4	"
26	JA3	"
27	JA2	"
28	JA1	"
29	JA0	"
30	JD0	Data line
31	JD1	"
32	JD2	"
33	JALP	Write protect
34	GND	Ground
35	GND	Ground
36	JACD1	Card detect
37	not used	
38	not used	
39	not used	
40	not used	
41	not used	
42	not used	
43	not used	
44	not used	
45	not used	
46	JA17	Address line
47	JA18	"
48	JA19	"
49	JA20	"
50	JA21	Address line
51	VCC	Vcc
52	VPP	Vpp
53	JA22	Address line
54	JA23	"
55	JA24	"
56	JA25	"
57	not used	
58	not used	
59	not used	
60	not used	
61	-JRG0	Register select
62	JAV	Card battery voltage detect
63	JAV	Card battery voltage detect
64	not used	
65	not used	
66	not used	
67	JACD2	Card detect
68	GND	Ground

11.10.2 The Card Interface

Each card connector has a separate interface device (COI100). This provides buffering of the system bus address and data lines (EA[0..19] and ED[0..7]) and control logic. The pinouts are as follows:

Pin	Signal	Description
1	GND	Ground
2	-OUTE	Not used
3	EA16	System bus address line
4	EA17	"
5	EA18	"
6	EA19	"
7	-JRB	Register select (input)
8	-JACE	Interface chip enable (input)
9	not used	
10	ALE	Address lines valid (input)
11	-JCPE	Interface power enable (input)
12	GND	Ground
13	not used	
14	JD3	Card data bus line
15	JD4	"
16	JD5	"
17	JD6	"
18	JD7	"
19	GND	Ground
20	-JCE01	Card enable (output)
21	JA10	Card address line
22	-JCE	Output enable for card
23	JA11	Card address line
24	GND	Ground
25	not used	
26	VDD	5V in
27	JA9	Card address line
28	JA8	"
29	JA13	"
30	JA14	"
31	JA17	"
32	JA18	"
33	JA19	"
34	GND	Ground
35	JA20	Card address line
36	JA21	"
37	-JWE	Card write enable
38	not used	
39	JA16	Card address line
40	JA15	"
41	not used	
42	JA12	Card address line
43	GND	Ground
44	JA22	Card address line
45	JA23	"
46	JA24	"
47	JA25	"
48	JRG0	Register select output
49	VDD	5V in
50	VDD	5V in
51	not used	
52	GND	Ground
53	JA7	Card address line
54	JA6	"
55	JA5	"
56	JA4	"
57	JA3	"
58	JA2	"
59	JA1	"
60	JA0	"
61	GND	Ground
62	JD0	Card data line
63	not used	
64	JD1	Card data line
65	JD2	"
66	-JCE02	not used
67	not used	
68	EA0	System bus address line
69	EA1	"

70	EA2	"
71	EA3	"
72	EA4	"
73	EA5	"
74	EA6	"
75	GND	Ground
76	VDD	5V in
77	-JCE12	Interface enable
78	VCCJC2	5V out for card
79	not used	
80	EA7	System bus address line
81	EA8	"
82	EA9	"
83	EA10	"
84	EA11	"
85	EA12	"
86	EA13	"
87	EA14	"
88	not used	
89	EA15	"
90	GND	Ground
91	not used	
92	ED0	System bus data line
93	ED1	"
94	ED2	"
95	ED3	"
96	ED4	"
97	ED5	"
98	ED6	"
99	ED7	"
100	VDD	5V in

11.10.3 The ROMP Register

Access to a PCMCIA card is controlled via the SPC ASIC's ROMP register:

Bit	Description
07	Ignored
06	Select register memory on both cards [1]
05..3	Ignored
02	Turn on programming voltage (+12V) to both cards [2]
01	Turn on +5V to card B
00	Turn on +5V to card A

Notes:

- [1] D6 must be 0 while programming a FLASH memory card.
- [2] D2 must be 0 before exiting a FLASH memory card programming sequence.

11.11 Serial Input/Output Interface

The serial input/output interface emulates the standard M8250B device. It may be programmed as either a primary or secondary port, with the SPC ASIC routing the serial interrupt output (SINT) to the appropriate IRQ (4 or 3) automatically.

The serial port connector is a 12-way sub-miniature D type with pinouts as follows:

Pin	Signal	Type	Pin	Signal	Type
1	DCD	Input	7	RTS	Input
2	RXD	Output	8	CTS	Input
3	TXD	Output	9	RI	Input
4	DTR	Output	10	VCC	
5	GND	Ground	11	GND	Ground
6	DSR	Input	12	GND	Ground

11.12 Printer Interface

The printer interface is Centronics compatible. The decode logic (including generation of the printer port interrupt, PPTI) is provided by the DVC ASIC.

The parallel printer pinouts are on a 22-way sub-miniature D type and are as follows:

Pin	Signal	Type	Pin	Signal	Type
1	Strobe*	Output	10	ACK*	Input
2	Data 0	Output	11	Busy	Input
3	Data 1	Output	12	Paper out	Input
4	Data 2	Output	13	Select*	Output
5	Data 3	Output	14	Autofeed*	Output
6	Data 4	Output	15	Error*	Input
7	Data 5	Output	16	Reset*	Output
8	Data 6	Output	17	Select	Output
9	Data 7	Output	18..22	Ground	

Notes:

* Means that the signal is active low.

11.13 Sound Generation

The SPC ASIC provides three sound outputs: the normal PC sound source (PCS) and two programmable sine wave generators (SWGs):

The normal PC sound source is the PCS signal, OUT2 of the 8253 which is ANDed with M8255 PB1. This is only enabled if both SWGs are disabled and uses pins SCA2 and SCB2 for output.

The SWGs are controlled by writing to SWG0 and SWG1 registers:

Register	Description
SWG0	SWG 0 divisor, LSB (DV0..7)
SWG0, D0..2	SWG 0 divisor, MSB (DV8..10)
SWG0, D3	SWG 0 Enable
SWG1	SWG 1 divisor, LSB (DV0..7)
SWG1, D0..2	SWG 1 divisor, MSB (DV8..10)
SWG1, D3	SWG 1 Enable (0=disable, 1=enable)

The output frequency is $1,250,000/n$, where n is the divisor, normally in the range 502..2009 (decimal), giving frequencies in the range 622.2 and 2490 Hz, nominal. The sine wave output is in 11.25 degree steps with 27 levels.

12. Miscellaneous

12.1 Serial Wake up

pc-3000 has the function to wake up by the serial communication signals.

12.1.1 Wake up by serial data/line.

[Procedure]

- Set the serial interrupt vector (0:0Ch*4 or 0:0Bh*4) to point ANYWHERE BUT THE INITIAL BIOS VECTOR.
- Unmask the relevant interrupt (IRQ 4: COM1 or IRQ3: COM2) of interrupt controller (8259).
- Enable the relevant communication port.(The method is mentioned later.)

[Note]

If you follow the above procedure, the PC-3000 can wake up by the interrupt from serial data/line input. If you set above procedure and turn off the machine, the serial buffer is powered up and the serial controller is enabled while PC-3000 is turned off so that the PC-3000 can wake up by the serial interrupt. Consequently, the battery life will be reduced.

We recommend that you mask the relevant interrupt and reset the interrupt vector to the default value which initial BIOS pointed when you exit the communication(i.e to go into the command menu or the communication setting up menu, etc.).

12.1.2. Wake up by RI (Ringing Indicator)

[Procedure]

- The serial interrupt vector (0:0Bh*4 or 0:0Ch*4) SHOULD point the INITIAL BIOS VECTOR.
- Unmask the relevant interrupt (IRQ 4: COM1 or IRQ3: COM2) of the interrupt controller (8259).

[Note]

If you follow the above procedure, the PC-3000 can wake up only by RI signal. Waking up by RI signal does not need to power the serial buffer/serial controller when the PC-3000 is turned off. Therefore this method can save the battery power than the method of 12.1.1 while the PC-3000 is turned off.

However RI coming from the external equipment can only wake up the machine. Hence, it is necessary for the application software to detect which events turned on the machine.

In order to detect the incoming RI in wake up procedure, it is necessary to enable the serial port and poll the RI bit through the serial controller RI. If the incoming RI is detected through the serial controller, the wake up is caused by the serial RI signal. Otherwise the wake up is caused by other events such as keypress.

12.1.3. Control the serial port

There are several ways to control the serial port and select the serial port as follows. Please refer to the section of '2.2 The Extended BIOS' regarding each Extended BIOS function, parameters or in details.

12.1.3.1 Enable/Disable the serial port

You can enable the serial port either by using 'System Setup' menu or by using 'Extended BIOS function' service.

[By the 'System Setup' menu]

You can enable/disable the serial port communication using 'Low-power mode' set function in the 'System Setup' menu as follows;

Enable : set 'Low-power mode' to OFF
Disable : set 'Low-power mode' to ON

[By the Extended BIOS function]

You can enable/disable the serial port communication using using 'Set low power mode' function in the Extended BIOS (XBS) services.

Enable : using 'Set low power mode' XBS function as follows;

```
MOV AX,8312h
MOV CX,0000h
INT 7Eh
```

This setting functions as same as the setting 'Low-power mode' to OFF in the 'System Setup' menu.

Disable : using 'Set low power mode' XBS function as follows;

```
MOV AX,8312h
MOV CX,0073h
INT 7Eh
```

This setting functions as same as the setting 'Low-power mode' to ON in the 'System Setup' menu.

Also you can enable/disable the serial communication independently by controlling the bit 0 of the Power control bits in the 'Set low power mode' Extended BIOS service.

12.1.3.2 Selecting the communication port

You can select the communication port either by using 'System Setup' menu or by using 'Extended BIOS function' service.

[Using 'RS-232C port settings...' in the 'System Setup']

Select the relevant communication port to COM1 or COM2 in the 'RS-232C port setting...' of the 'System Setup'

[Using 'Set serial port (COM1/COM2) destination' XBS function]

```
MOV AX,8E07h
MOV CL,xx          ; xx; 00=disable, 01=COM1, 02=COM2
INT 7Eh
```

12.1.4. Turn off the machine

PC-3000 can be turned off by pressing 'Fn+ESC' or turned off automatically unless there is keypress for a specific period of time set in 'Setup Menu'. Also it is possible to turn PC-3000 off by program with using 'Initiate power down' Extended BIOS service as follows;

```
MOV AX,830Eh
INT 7Eh
```

12.1.5 Turn ON/OFF Sample

Following sequence is just an example for turning on/off the machine with using above method of 12.1.2

```
[Exit from communication.]
|
Mask the serial IRQ of the interrupt controller
|
Set the serial interrupt vector to the default.
|
Unmask the serial IRQ
|
Turn off
|
(Coming RI)-->
|
Enable the serial power
|
Check RI coming.
```

If RI is coming, the wake up is caused by the serial. PC-3000 may go into communication procedure.

or

If RI is not coming, the wake up is caused by other events such as keypress.