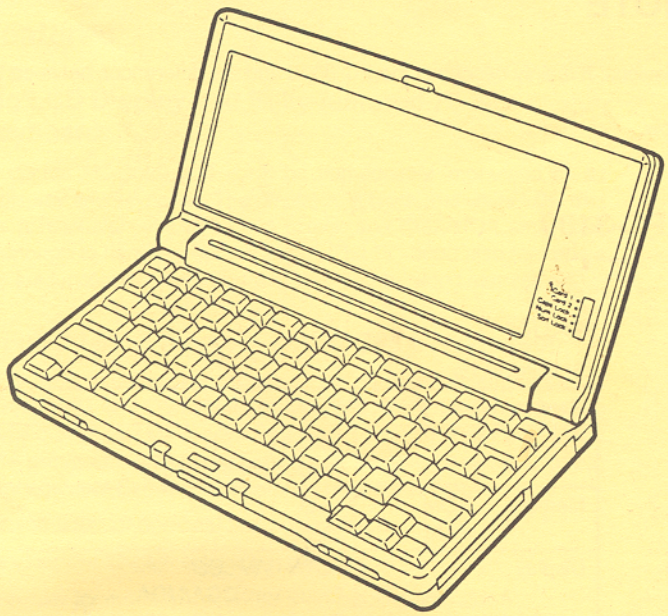
SHARP SERVICE MANUAL

CODE: 00ZPC3000SM/E



PALMTOP COMPUTER

PC-3000
MODEL PC-3100

OPTION: CE-301F
CE-301CB
CE-302CB
CE-303CB

CONTENTS

SHARP CORPORATION

NOTE

This Service Manual is for the PC-3000/PC-3100 and their peripheral devices. It mainly describes the PC-3000 and the differences between the two models are added.
The differences between the PC-3000 and the PC-3100 are shown below.

1. Differences between the PC-3000 and the PC-3100

(1) Hardware specifications

PC-3000

Specifications

Hardware (Main PWB: DUNTK1289RHZZ)	
CPU	80C88A Clock Speed: 10MHz
Memory ROM RAM	1MB 1MB
Display	FSTN B/W LCD Emulation: CGA/MDA Resolusion: 640x200 pixels
Keyboard	Qwerty 77 keys
I/O ports	Serial (RS-232C) interface port x 1 Parallel interface port x 1 PCMCIA 1.0 IC card x 2 Expansion bus port for 3.5" FDD unit
Dimension (W x D x H)	222 x 112 x 25.4 mm (8.8" x 4.4" x 1.0")
Weight	Approx. 1lb. (480 g)
Power supply	AA batteries x 3, Lithium battery x 1 Optional AC adaptor

PC-3100

Specifications

Hardware (Main PWB: DUNTK1292RHZZ)	
CPU	80C88A Clock Speed: 10MHz
Memory ROM RAM	1MB 2MB
Display	FSTN B/W LCD Emulation: CGA/MDA Resolusion: 640 x 200 pixels
Keyboard	Qwerty 77 keys
I/O ports	Serial (RS-232C) interface port x 1 Parallel interface port x 1 PCMCIA 1.0 IC card x 2 Expansion bus port for 3.5" FDD unit
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Weight	Approx. 1lb. (480 g)
Power supply	AA batteries x 3, Lithium battery X 1 Optional AC adaptor

(2)Mechanism

	PC-3000	PC-3100
DECORATION PANEL	0 G M 4 0 1 5 4 1 0 1 / /	0 G M 4 0 1 5 8 1 0 1 / /
CAB-C	0 G M 7 3 1 5 4 1 0 4 / /	0 G M 7 3 1 5 8 1 0 1 / /
PACKING CASE	G version 0 G M 6 1 5 0 1 0 9 6 / / Other version 0 G M 6 1 5 0 1 0 9 5 / /	G version 0 G M 6 1 5 0 1 0 9 9 / / Other version 0 G M 6 1 5 0 1 0 9 8 / /
PATING CABEL	0 G M 6 0 2 0 2 8 1 3 / /	0 G M 6 0 2 0 2 8 3 1 / /
F mark self-declaration	0 G M 6 0 2 0 2 8 1 7 / /	0 G M 6 0 2 0 2 8 3 2 / /
MASTER PACKING CASE	0 G M 6 1 5 0 1 0 9 4 / /	0 G M 6 1 5 0 1 0 9 7 / /

CHAPTER 1. OUTLINE OF THE PC-3000

1. Features

1) Big LCD Display and Fully-featured 77-key Keyboard

Open up the PC-3000 and you'll be immediately impressed by its large display and keyboard. The display is a black and white LCD that boasts a resolution of 640 × 200 pixels, and CGA/MDA emulation. Wide enough to handle a spread sheet. The PC-3000 also features a 77-key full-functioning keyboard that your fingers won't stumble on.

2) A Full 2 MB of Memory and 80C88A Processor

The PC-3000 features two megabytes of system memory: 1MB of RAM and 1MB of ROM. That's a size that many laptop and some desktops don't boast of. Together with such capacity, there's a 10MHz 80C88A processor, giving you high-speed access. Personal Information Management Software is also provided as standard.

- Address book for personal and business data
- Calculator for 12-digit calculation with memory
- Scheduler for monthly/weekly/daily scheduling with alarm
- Editor for making notes and organizing reports
- Spreadsheet for processing business data
- Clock
- To-do list for arranging your jobs.
- File Manager for running applications and managing files without struggling with DOS commands

3) Full Expansion Capabilities

Memory expansion comes from dual IC card ports which increase the PC-3000's RAM and ROM, and are lockable for convenience and safety. Any work done on the road can be instantly transferred to your main computer via an RS-232C. In addition, the PC-3000 is fully IBM® PC compatible.

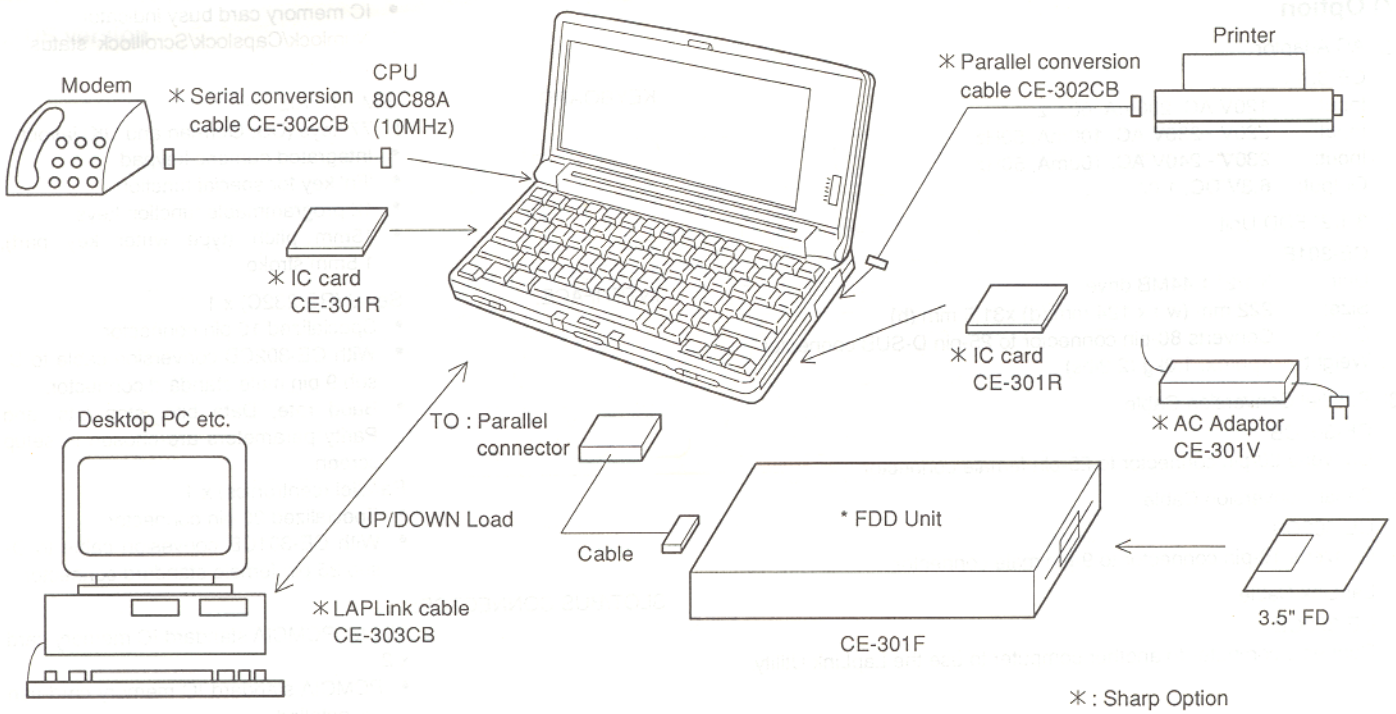
4) This Computer Speaks a standard of 7 Languages

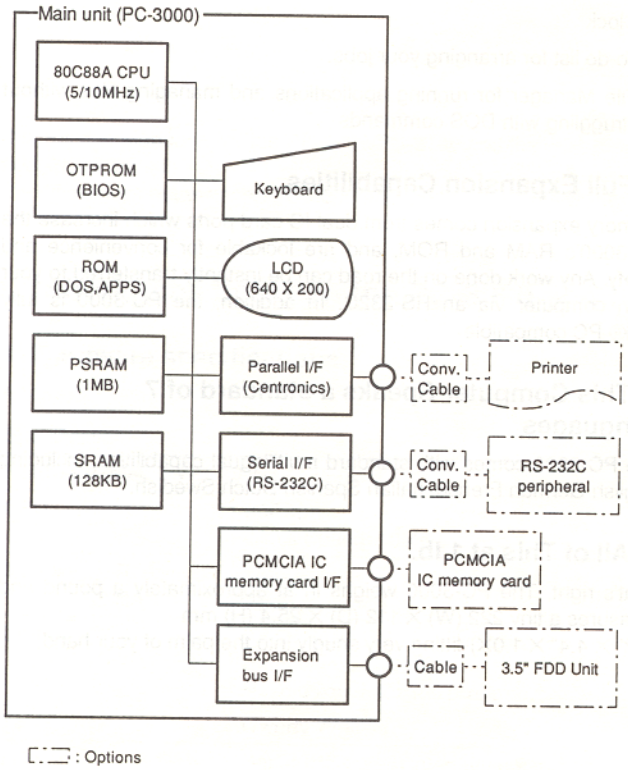
The PC-3000 comes with standard multilingual capabilities, including English German French, Italian Spanish Dutch Swedish.

5) All of This at 1 lb.

That's right. The PC-3000 weighs in at approximately a pound and measures a tiny 222 (W) × 112 (D) × 25.4 (H) mm
(8.8" × 4.4" × 1.0X)-fitting very snugly into the palm of your hand!

6) System configuration





7) Option

① AC Adaptor

CE-301V

Input: 120V AC, 200mA, 60 Hz
Input: 220V - 230V AC, 100mA, 50Hz
Input: 230V - 240V AC, 100mA, 50Hz
Output: 6.3V DC, 1.0A

② 3 1/2" FDD Unit

CE-301F

Unit: 3 1/2" 1.44MB drive
Size: 222 mm (w) x 124 mm (d) x31.5 mm (h)
Cable: Converts 80-pin connector to 25-pin D-SUB connector
Weight: Approx. 1.0kg (2.2lbs)

③ Parallel Conversion Cable

CE-301CB

Converts 20-pin connector to 25-pin female connector

④ Serial Conversion Cable

CE-302CB

Converts 10-pin connector to 9-pin male connector

⑤ LapLink Cable

CE-303CB

Connects computer to another computer to use the LapLink Utility.

2. Specification

1) Hardware

CPU: 80C88 (10/5MHz)
- Clock speed can be changed in Setup screen.

CO-PROCESSOR: N/A

ROM: 1M byte Mask ROM x 1
- Contents: MS-DOS, Application, Laplink, DIAG, ROM libraries

128K byte OTPROM x 1
- Contents: IPL, Self Test, BIOS, Video BIOS

RAM: 1M byte standard
- 4M bit PS-RAM x 2
- 640K byte for conventional, 384K byte for RAM disk or Extended memory
- LIM/EMS 4.0 support
- Bus width: 16 bit

128K byte SRAM
- 1M bit SRAM x 1
- 16K byte for video memory, 3K byte for system, 109K byte for RAM disk

DISPLAY: FSTN (Film Super Twisted Nematic) LCD w/o backlight
- Resolution: 640 x 200 pixels
- CGA/MDA compatible
- 4 gray shades
- Viewing area: 6.8" x 2.6"
- Aspect ratio: 1:2
- Dot pitch: 0.27mm x 0.33 mm
- Contrast is adjustable by Fn key function

Static LCD
- IC memory card busy indicator
- Numlock/Capslock/Scrolllock status indicator

KEYBOARD: IBM 101/102 like keyboard layout
- 77 keys (US, German and UK) layout
- Integrated numeric keypad
- 'Fn' key for special function
- 12 programmable function keys
- 15mm pitch (type writer key part), 1.5mm stroke

INTERFACE: Serial (RS-232C) x 1
- Specialized 10 pin connector
- With CE-302CB conversion cable to D-sub 9 pin male standard connector.
- Baud rate, Data bits, stop bits, and Parity parameters are chosen in setup screen.

Parallel (centronics) x 1
- Specialized 20 pin connector
- With CE-301CB convesion cable to D-sub 25 pin female standard connector

SLOT/BUS CONNECTOR:

Slot for PCMCIA standard IC memory card x 2
- PCMCIA standard IC memory card can be installed.

Expansion Bus connector x 1
- CE-301F 3.5"FDD unit can be connected with FDD cable.

POWER SUPPLY: AA dry battery x 3
- Main battery

Lithium battery x 1
- for SRAM memory backup
- Provides backup power while changing the AA battery

CE-301V AC adaptor
- Specified adaptor for each destination
- Output: 6.3V DC
- AC cord is not detachable from AC adaptor.

BATTERY LIFE: 30 hours
- LCD contrast medium, without options.

POWER SAVE FUNCTION:

Automatic clock stop
- No activities make CPU clock stop automatically.

Automatic power down
- No key input for certain period causes automatic power down.

LOW BATTERY ALARM: 1st-step:
When a battery is discharged to preset level, LOW BATTERY warning message appears on the screen and CPU speed is decreased.

2nd-step:
When a battery is almost empty, FLAT BATTERY warning message appears on the screen and turn the power off automatically.

POWER CONSUMPTION:
Typ. 0.4 W (without options)

Key board Layout

a) US version

a) US version

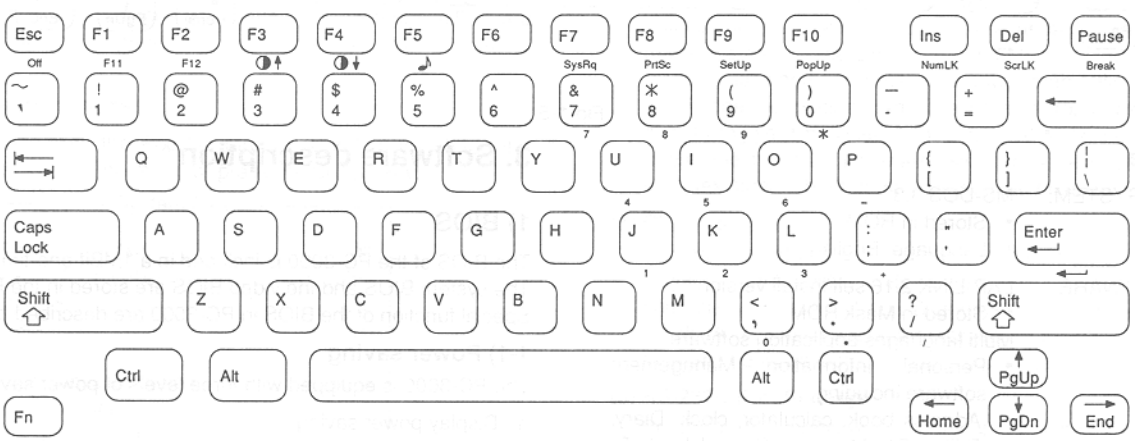


Fig.1-3

2) Mechanical

CONNECTORS:
External connectors for:

Serial interface:	Specialized 10 pin connector
Parallel interface:	Specialized 20 pin connector
AC adaptor:	2 conductor phone jack
Expansion bus:	80 pin connector

SLOTS: Slots for; PCMCIA standard IC memory card x 2

LEVERS: Levers for; PCMCIA IC card removal x 2

SWITCHES: Reset switch (button switch)
IC memory card lock switch x 2

DIMENSIONS:
4.4"(D) x 8.8"(W) x 1.0"(H)
112mm(D) x 222mm(W) x 25.4mm(H)

WEIGHT: 450 g
(Main unit with battery)

b) UK version

b) UK version

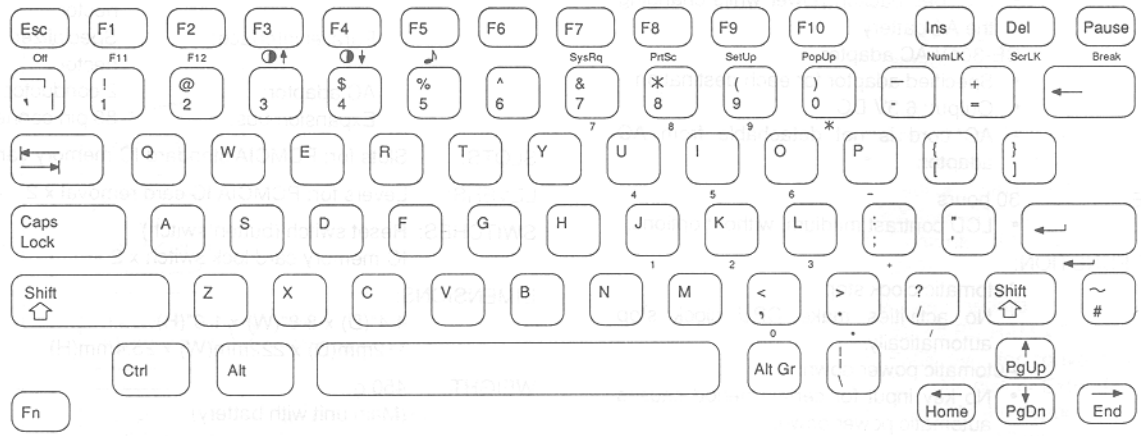


Fig.1-4

c) German version

c) German version

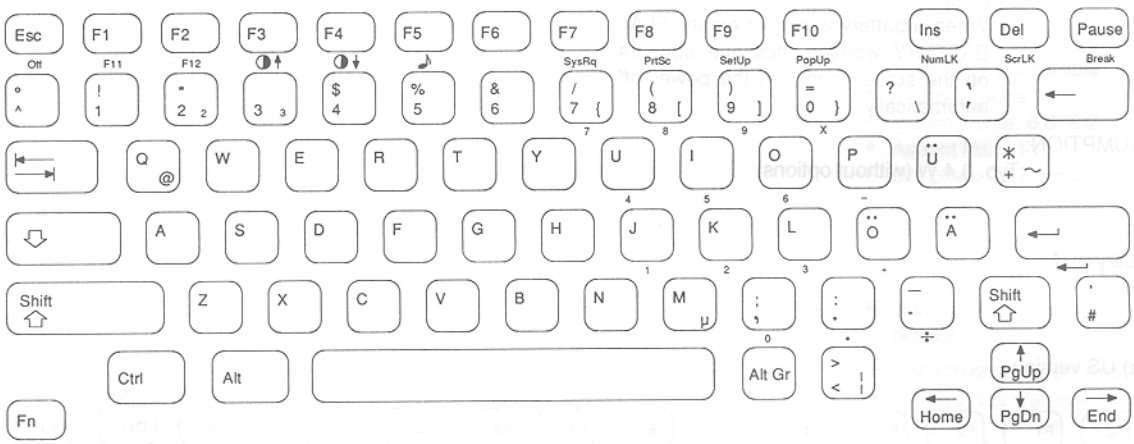


Fig.1-5

3) Software

OPERATING SYSTEM: MS-DOS 3.3
- Stored in ROM
- Language: English

BUILT-IN SOFTWARE: LAP-LINK 2.16 self install version
- Stored in Mask ROM

Multi languages application software
- Personal Information Management software including;
  Address book, calculator, clock, Diary, Editor, File Manager, Spreadsheet, To Do List
- Stored in Mask ROM
- Languages; English, German, French Intalic, Spanish, Dutch, Swedish

4) Operational and storage range

Operational range:
50 to 95 degrees F
10 to 35 degrees C
20 to 80% humidity (Non-condensing)

Storage range:
–4 to 140 degrees F
–20 to 60 degrees C
10 to 90% humidity (non-condensing)

3. Software description

1) BIOS

The BIOS of the PC-3000 is included in a 1MBit one-time ROM. The system BIOS and the video BIOS are stored in the ROM. Special function of the BIOS in PC-3000 are described below:

1-1) Power saving

The PC-3000 is equipped with three levels of power saving.

① Display power saving

② System power saving

These power saving functions are performed with the time-out values set by SETUP. The system power saving can be also executed by key input. Some application software may not work correctly with system power saving function. If there are any problems in the power saving function, Please disable the function by SET_UP.

1-2) Automatic setting of hardware

The PC-3000 hardware setting is performed for the following items.

① Built-in CGA mode setting

② Display adapter setting

③ Each device I/O port setting

④ FDD assignment (When FDD is set)

⑤ Built-in memory setting

The following items are automatically detected and proper settings are made automatically.

① FDD presence

② FDD type

③ Main memory and expansion memory capacity

When no FDD is connected, BIOS level emulation is performed. Then the machine works as if two FDDs are connected without disk insertion.

1-3) ROM disk

To use ROM disk, set Drive C to ROM disk in hardware installation. With the ROM disk, only the following three items can be executed.

① MS-DOS installation

② Diag. program execution

③ Setup execution

④ Muti languages application software

1-4) Special functions with key operation

- Fn + F3: LCD contrast is dark.
- Fn + F4: LCD contrast is bright.
- Fn + F5: KEY click ON/OFF.
- Fn + F10: Popup program excution.
- Fn + F9: Setup program excution.

2) Setup

2-1) Setting up the Machine

You can configure various aspects of the hardware by selecting menu options as follows. The changes you make will remain until either you change them again, or perform a cold boot (i.e. lose all battery power).

To set up the hardware:

- Select Options from the Pop Up Menu and select the Setup the machine option from the menu or press the Set Up key:

System Setup

Low-power mode	On
Power down delay . . .	2 minutes
Keyclick	On
All sounds	On
Screen inverse	
Microprocessor speed	10 MHz
Character set	Default
RS-232C port settings . . .	

This shows the current setting for each setup option, other than the RS-232C port.

- To change a setting, select it by typing its initial letter OR move the highlight to it and press Enter.
- Once you have defined the setup you want, press Es: to store it and return to the Options menu. The changes take effect immediately.

Each option will now be described in turn.

(1) Low Power Mode

Normally, the computer switches off the processor when there is no processing to perform. This is low power mode, and is used to maximize battery life. However, certain badly-behaved third party programs may not operate correctly with low power mode selected, as this also stops the timer ticks which such programs may rely on.

To disable low power mode, select the Low-power mode option to toggle the setting to Off. To restore normal power handling, toggle it back to On.

Caution: If you disable low power mode, the batteries will run down very quickly!

(2) Power Down Delay

The computer will normally turn itself off to conserve battery power, if it has been waiting for keyboard input for more than 5 minutes. To control power down, select the Power down delay option and choose an option (0, 1, 2 or 5 minutes) from the menu; 0 means do not power down. For example, you might select 1 minute to maximize battery life.

(3) Keyclick

Normally, all keyboard keys sound a click via the speaker when you press them, but you can toggle this off or on again by selecting the Keyclick option or by pressing Fn-F5. If the keys don't click with Keyclick set to On, check the All sounds setting.

(4) All Sounds

The computer normally uses audible signals to warn you of errors, indicate that a clock alarm is ringing and for keyclicks, but you can toggle these all between Off and On by selecting the All sounds option. For example, you might be working in a place where the noise is intrusive, such as a library.

(5) Screen Inverse

The computer screen normally shows black text on a white background. Select the Screen inverse option to toggle between this and white text on a black background. (The change is made immediately.)

(6) Microprocessor Speed

The computer can operate at two clock speeds: 5MHz and 10MHz. These have nothing to do with time keeping, they dictate the speed at which the microprocessor executes programs i.e. at 10MHz, programs execute up to twice as fast. The computer normally operates at the slower speed, 5MHz, as this is fast enough for most uses and consumes less power than 10MHz operation.

To change the clock speed, select the Microprocessor speed option, to toggle it between 5 MHz and 10 MHz. For example, you might select 10 MHz if you are using the Worksheet with a large or complex spreadsheet, to reduce the time taken to recalculate.

(7) Character Set

A character set is the range of characters that the computer displays for each ASCII code (0 to 255). The computer has two character sets: Default and Scandinavian, which are listed in Appendix A. To switch character sets, select the character set option, to toggle between Default (International) and Scandinavian.

(8) RS-232C Port Settings

Before using a serial port, you must check that it is set up to suit the connected device:

RS-232C Port

Baud rate . . .	9688
Parity . . .	None
Data bits	8
Stop bits	1
Mouse of port	COM1

CHAPTER 2. Disassembly and assembly

This chapter describes mainly on the disassembly procedures. For reassembly procedures, reverse the disassembly procedures. When special care is required for reassembly, [Note for reassembly] is given.

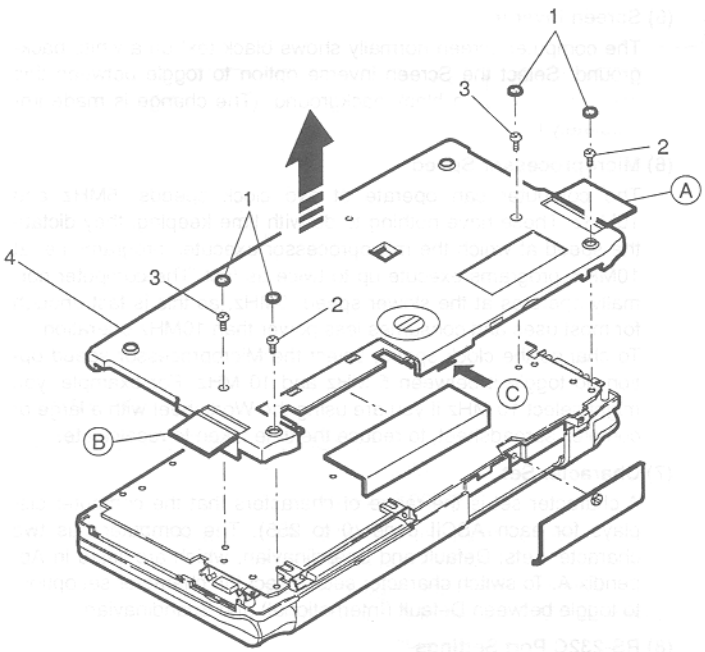
☆ [General notes]

- Before starting disassembly, remove all optional and built-in batteries connected with the body. When disconnecting, be sure to hold the sides of the connector, and never pull the lines. Otherwise the line may be broken.
- For easy and simple replacement of units and parts, explanations will be omitted.

1. Upper/lower cabinets disassembly

Disassembly

1) With the LCD panel closed, put the unit upside down.
2) Remove four rubber pins ①.
3) Remove two screws ② and two screws ③.
4) Remove lower cabinet ③ from upper cabinet ④.



[Note]

- To open the cabinet bottom, insert a mini-screwdriver ⊖ into the center portion Ⓒ in the rear side with connector covers Ⓐ and Ⓑ for serial and parallel and open it.
- Be careful to the speaker cable attached to the cabinet bottom.

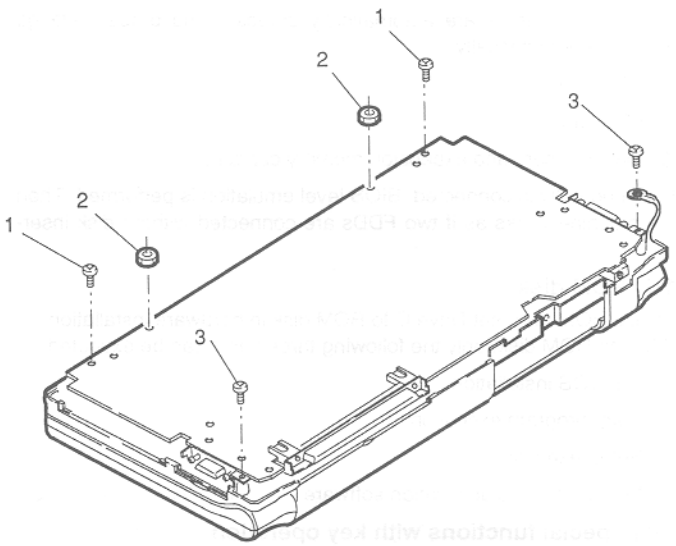
2. Main PWB disassembly

Preparations

Refer to Rep.1.

Disassembly

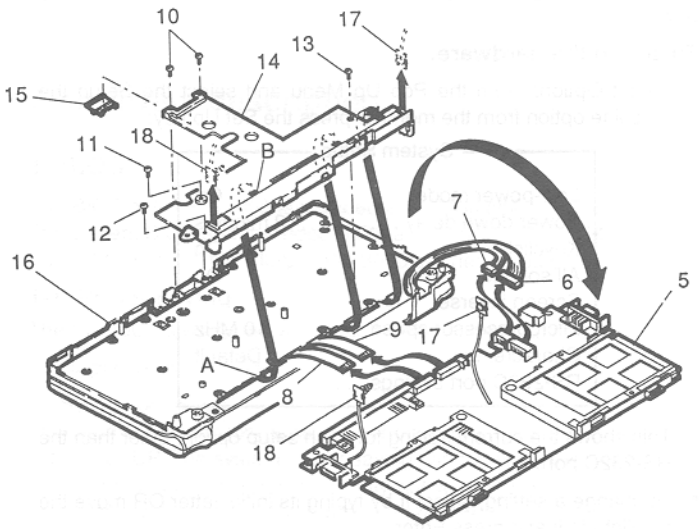
1) Remove two screws ①, two Nut ②and two screws ③.



[Note]

- When removing nut ②, be careful not to scratch the pattern.

2) Lift main PWB ⑤ and reverse it.
3) Pull out LCD cables ⑥ and ⑦.
4) Remove connectors ⑧ and ⑨.
5) Remove two screws ⑩ and screws ⑪, ⑫, and ⑬.
6) Remove battery cover ⑭ and open/close knob ⑮ from upper cabinet ⑯.



7) Remove battery terminal ⊕ ⑰ and battery terminal ⊖ ⑱ from battery cover ⑭.

[Note for reassembly]

- Insert three pawls in section Ⓐ of the keyboard into the holes in battery cover ⑭.

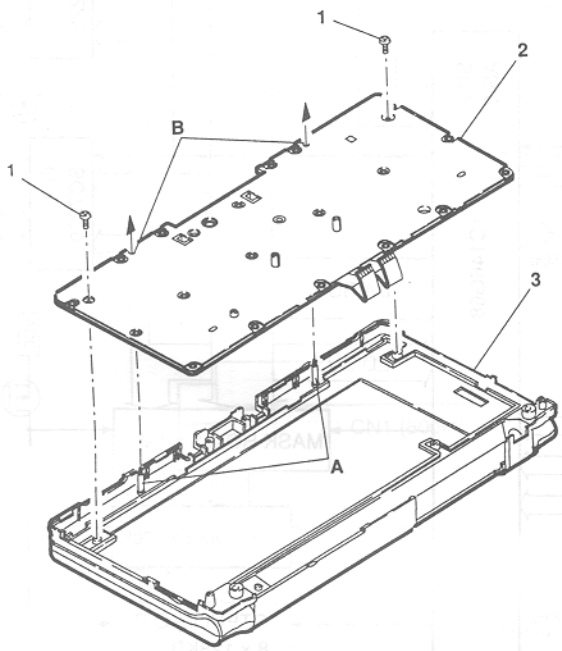
3. Keyboard disassembly

Preparations

Refer to Rep. 1, 2.

Disassembly

1) Remove two screws ①.
2) Remove keyboard ② from upper cabinet ③.



[Note for reassembly]

- Insert projected section Ⓐ of upper cabinet ③ into hole Ⓑ in keyboard ②.

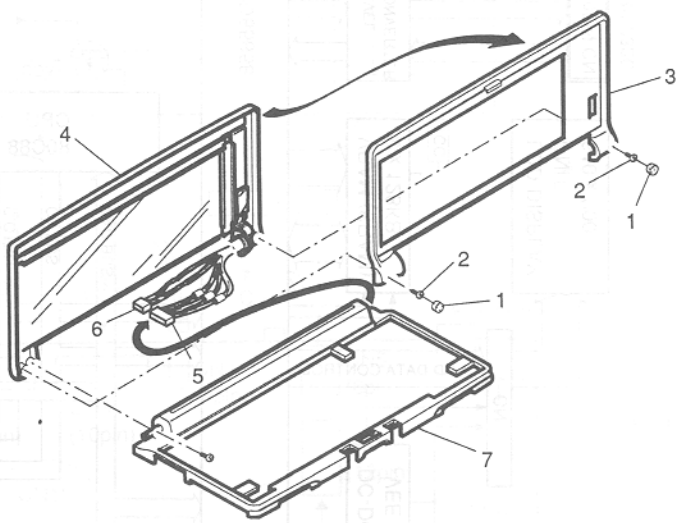
4. LCD disassembly

Preparation

Refer to Rep. 1, 2-2) to 3).

Disassembly.

1) Remove two rubber pins ① and two screws ②.
2) Remove display lower cabinet ③ from display upper cabinet ④.
3) Pull out LCD cables ⑤ and ⑥ from upper cabinet ⑦, and remove the display section from upper cabinet.



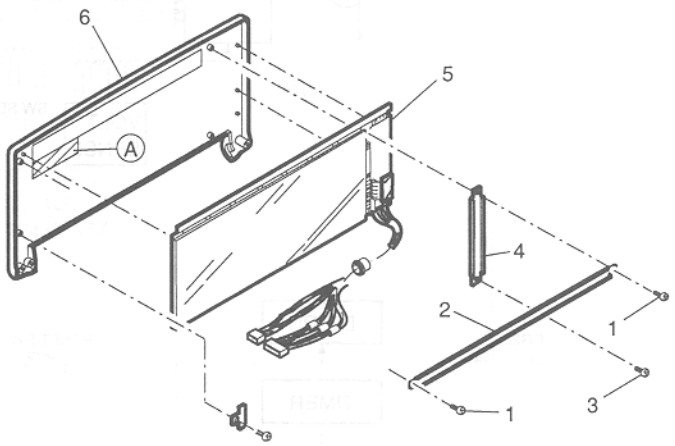
4-1. LCD panel disassembly

Preparation

Refer to Rep. 1, 2-1) to 3), and 4.

Disassembly.

1) Remove two screws ①, and remove LCD angle ②.
2) Remove screw ③ and LCD angle ④.
3) Remove LCD unit ⑤ from display upper cabinet ⑥.

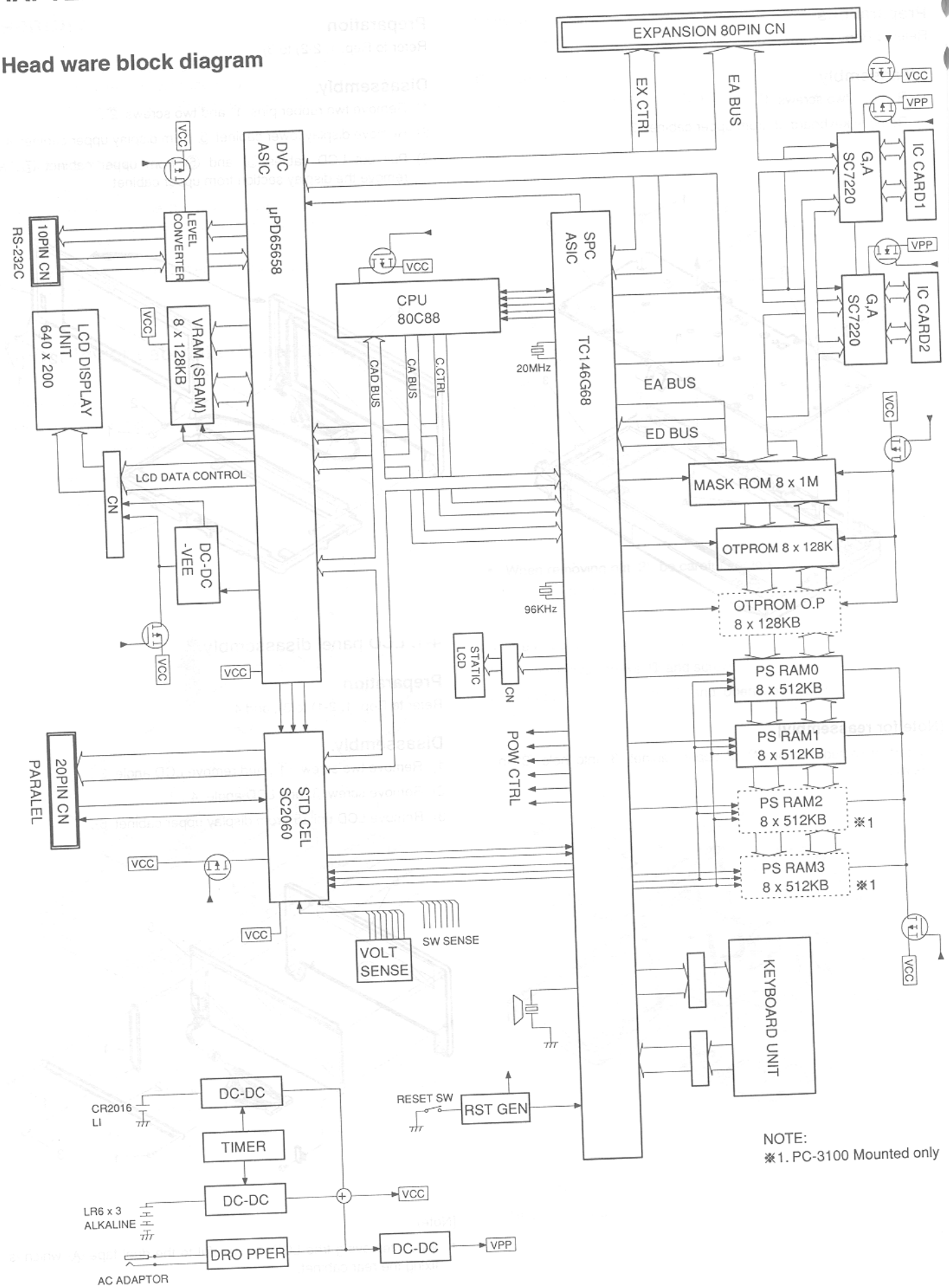


[Note]

- When removing trhe LCD, be careful to the dual tape Ⓐ which is fixing the rear cabinet.

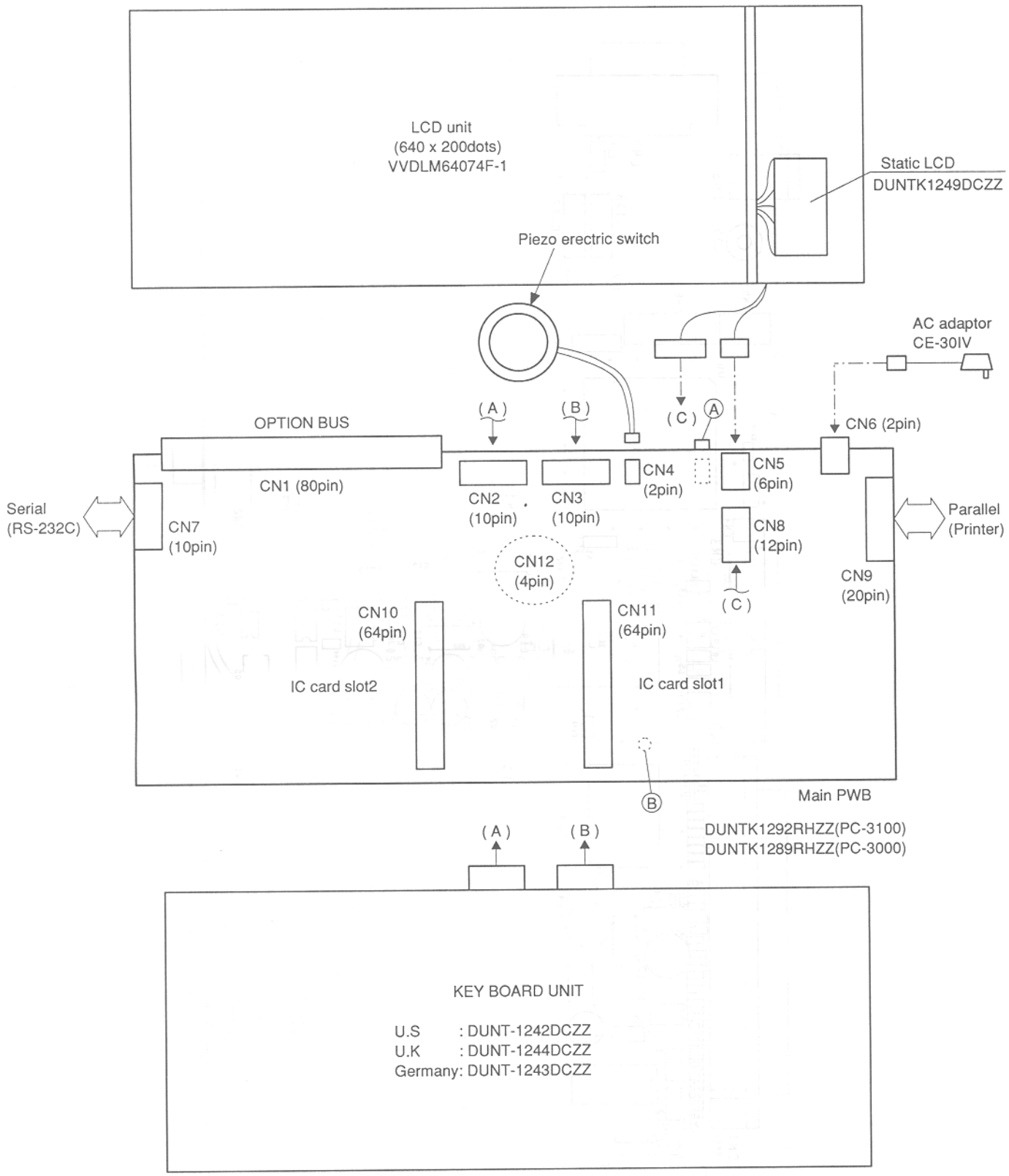
CHAPTER 3. SYSTEM BLOCK DIAGRAM

1. Head ware block diagram



NOTE:
※1. PC-3100 Mounted only

2. Unit block diagram



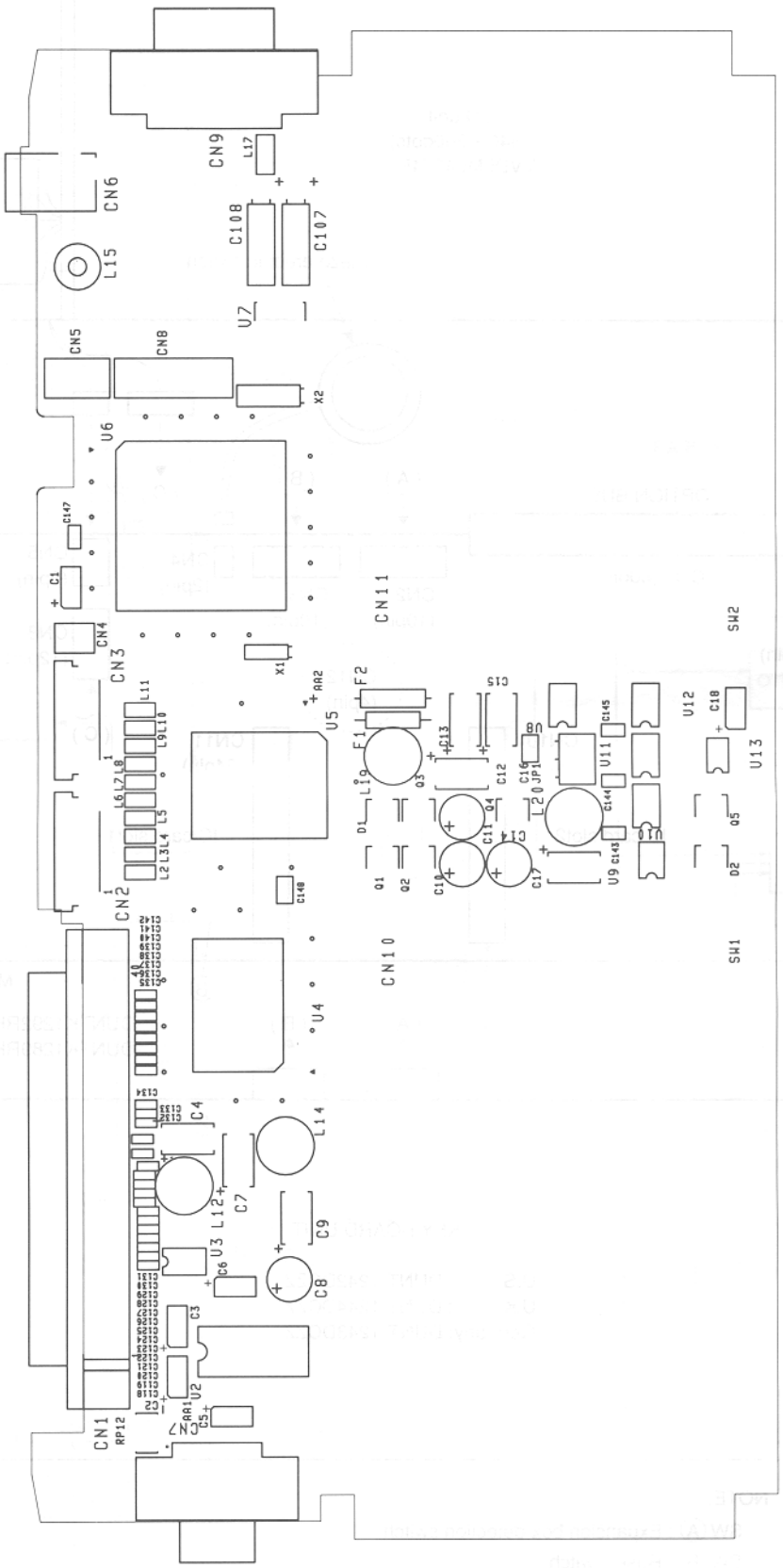
NOTE:

SW Ⓐ : Expansion box detection switch

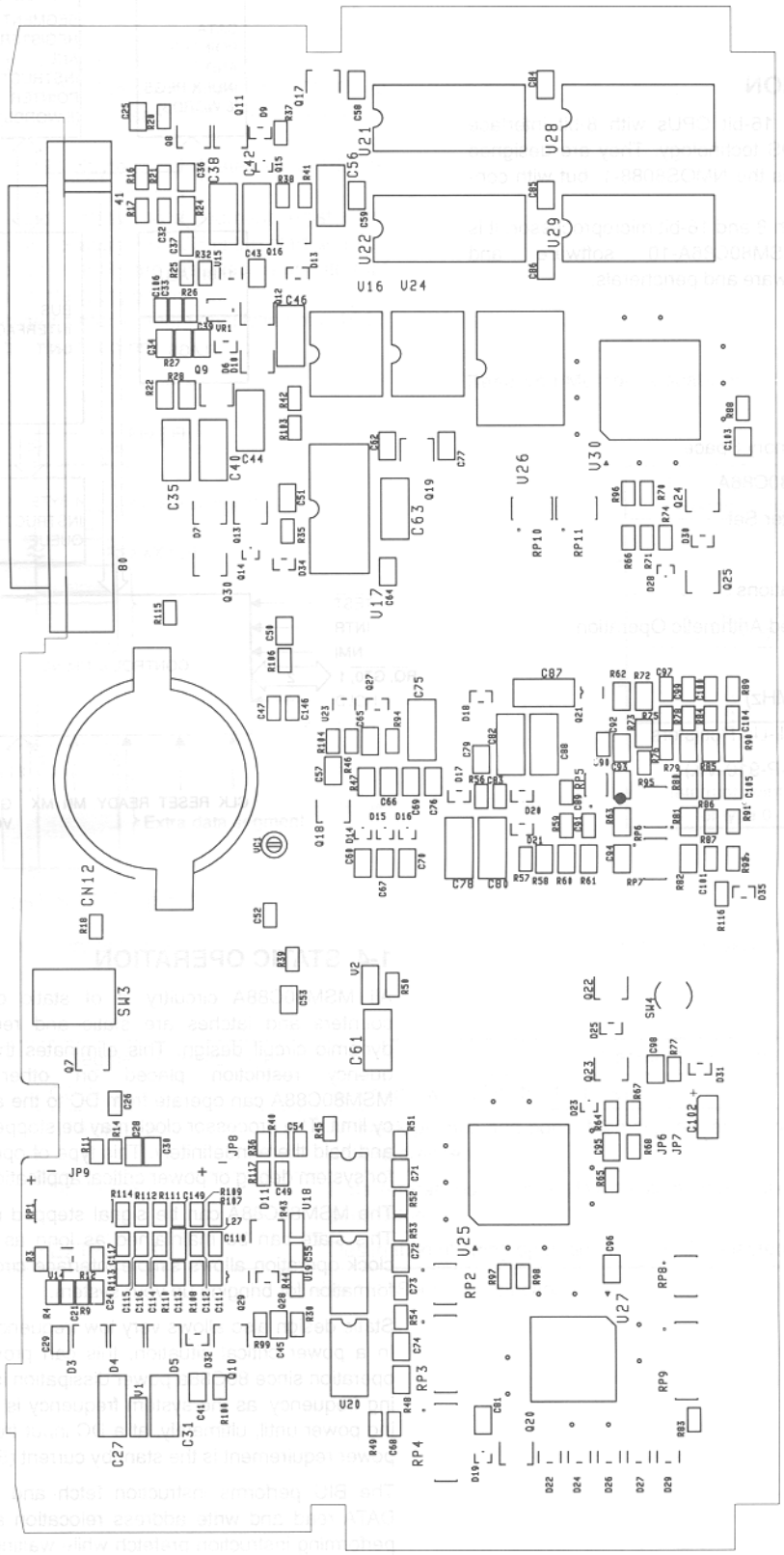
SW Ⓑ : Reset switch

3. Main PWB layout

(1) Top view



(2) Bottom view



CHAPTER 4. HARDWARE DESCRIPTION

1. CPU (MSM80C88A)

1-1. GENERAL DESCRIPTION

The MSM80C88A-10 are internal 16-bit CPUs with 8-bit interface implemented in Silicon Gate CMOS technology. They are designed with the same processing speed as the NMOS8088-1, but with considerably less power consumption.
The processor has attributes of both 8 and 16-bit microprocessor. It is directly compatible with MSM80C86A-10 software and MSM80C85A/MSM80C85A-2 hardware and peripherals.

1-2. FEATURES

- 8-Bit Data Bus Interface
- 16-Bit Internal Architecture
- 1 Mbyte Direct Addressable Memory Space
- Software Compatible with MSM80C86A
- Internal 14 word by 16-bit Register Set
- 24 Operand Addressing Modes
- Bit, Byte, Word and String Operations
- 8 and 16-bit Signed and Unsigned Arithmetic Operation
- From DC to 10 MHz Clock Rate
- Low Power Dissipation (10 mA/MHz)
- Bus Hold Circuitry Eliminates Pull-Up Resistors
- 56 pin(L)-V Plastic QFP (QFP56-P-910-VK)

1-3. FUNCTIONAL BLOCK DIAGRAM

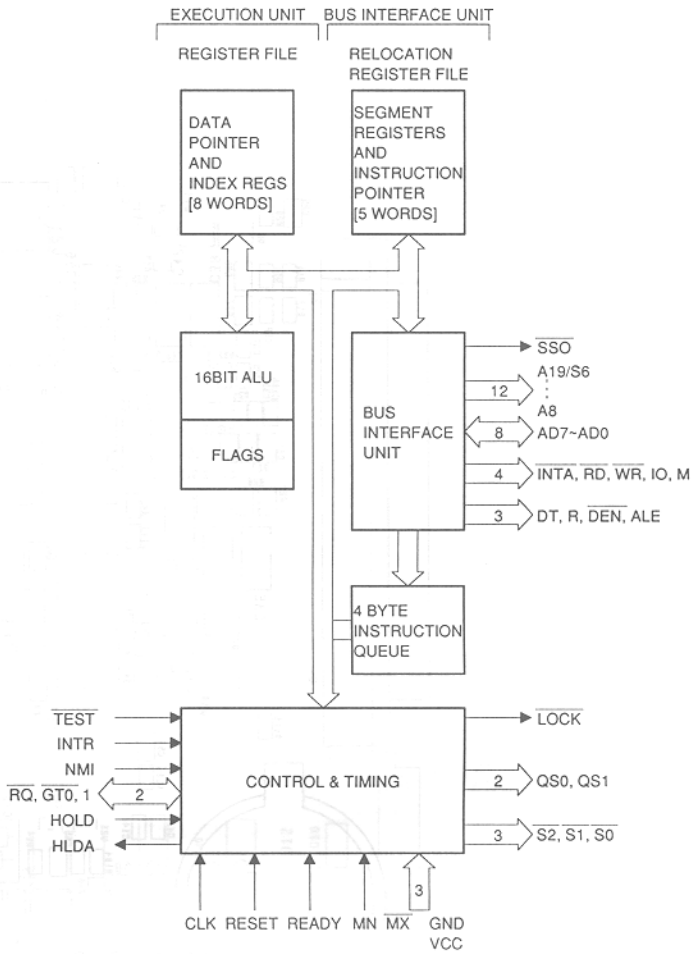


Fig.1-1 Block diagram

1-4. STATIC OPERATION

All MSM80C88A circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The MSM80C88A can operate from DC to the appropriate upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The MSM80C88A can be signal stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C88a power dissipation is directly related to operating frequency. as the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the MSM80C88A power requirement is the standby current (500 µA maximum).

The BIU performs instruction fetch and queueing, operand fetch, DATA read and write address relocation and basic bus control. By performing instruction prefetch while waiting for decoding and execution of instruction, the CPU's performance is increased. Up to 4-bytes fo instruction stream can be queued.
EU receives pre-fetched instructions from the BIU queue, decodes and executes instructions and provides an un-relocated operand address to the BIU.

1-5. FUNCTIONAL DESCRIPTION

(1) GENERAL OPERATION

The internal function of the MSM80C88A consist of a Bus Interface Unit (BIU) and an Execution Unit (EU). These units operate mutually but perform as separate processors.

(2) MEMORY ORGANIZATION

The MSM80C88A has a 20-bit address to memory.
Each address has 8-bit data width. Memory is organized 00000H to FFFFFH and is logically divided into four segments: code, data, extra data and stack segment.
Each segment contains up to 64 Kbytes and locates on a 16-byte boundary. (Fig. 3a)
All memory references are made relative to a segment register according to a select rule. Memory location FFFF0H is the start address after reset, and 00000H through 003FFH are reserved as an interrupt pointer. There are 256 types of interrupt pointer;
Each interrupt type has a 4-byte pointer element consisting of a 16-bit segment address and a 16-bit offset address.

Memory Organization

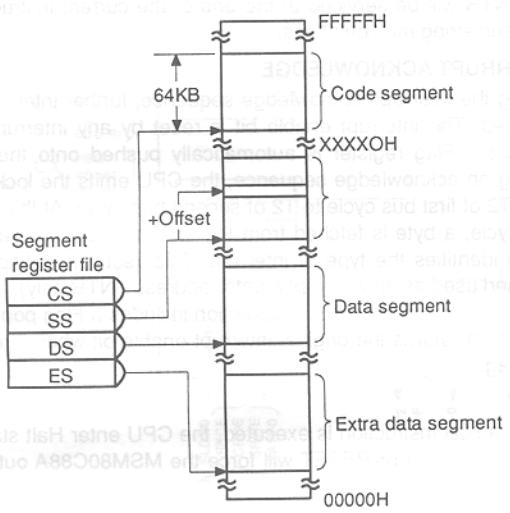


Fig.1-2 Memory organization

Reserved Memory Locations

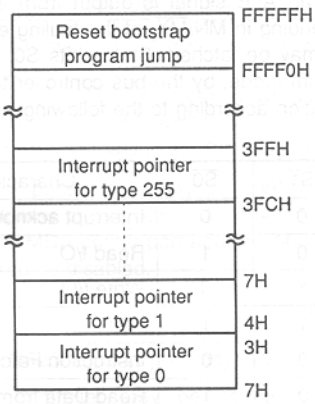


Fig.1-3 Reserved Memory Locations

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

Table 1-1. Segment selection

(3) MINIMUM AND MAXIMUM MODES

The MSM80C88A has two system modes: minimum and maximum. When using the maximum mode, it is easy to organize a multiple-CPU system with the MSM82C88 Bus Controller which generates the bus control signal.

When using the minimum mode, it is easy to organize a simple system by generating the bus control signal itself. MN/$\overline{MX}$ is the mode select pin. Definition of 24-31, 34 pin changes depends on the MN/$\overline{MX}$ pin.

(4) BUS OPERATION

The MSM80C88A has a time multiplexed address and data bus. If a non-multiplexed bus is desired for the system, it is only needed to add the address latch.

A CPU bus cycle consists of at least four clock cycles: T1, T2, T3 and T4. (See Fig.1-4)

The address output occurs during T1, and data transfer occurs during T3 and T4. T2 is used for changing the direction of the bus during read operation. When the device which is accessed by the CPU is not ready to data transfer and send to the CPU "NOT READY" is indicated TW cycles are inserted between T3 and T4.

When a bus cycle is not needed, T1 cycles are inserted between the bus cycles for internal execution.

At the T1 cycle an ALE signal is output from the CPU or the MSM82C88 depending in MN/$\overline{MX}$. at the trailing edge of an ALE, a valid address may be latched. Status bits S0, S1 and S2 are uased, in maximum mode, by the bus controller to recognize the type of bus operation according to the following table. (See Table 1-2)

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Table 1-2. Status bits selection

Status bit S3 through S6 are multiplexed with A16 ~ A19, and therefore they are valid during T2 through T4. S3 and S4 indicate which segment register was selected on the bus cycle, according to the following table. (See Table 1-3)

S4	S3	Characteristics
0 (LOW)	0	Alternate Data (Extra Segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

Table 1-3 S5 indicates interrupt enable Flag.

(5) I/O ADDRESSING

The MSM80C88A has a 64 Kbyte I/O. When the CPU accesses an I/O device, address A0 ~ A15 are in same format as a memory access, and A16 ~ A19 are low.

I/O ports address are same as four memory.

1-6. EXTERNAL INTERFACE

(1) RESET

CPU initialization is executed by the RESET pin.

The MSM80C88A's RESET High signal is required for greater than 4 clock cycles.

The rising edge of RESET terminates the present operation immediately. The falling edge of RESET triggers an internal reset requence for approximately 10 clock cycles. After internal reset sequence is finished, normal operation begins from absolute location FFFF0H.

(2) INTERRUPT OPERATIONS

The interrupt operation is classified as software or hardware, and hardware interrupt is classified as nonmarkable or maskable.

An interrupt causes a new program location which is defined by the interrupt pointer table, according to the interrupt type. Absolute location 00000H through 003FFH is reserved for the interrupt pointer table. The interrupt pointer table consists of 256-elements. Each element is 4 bytes in size and corresponds to an 8-bit type number which is sent from an interrupt request device during the interrupt acknowledge cycle.

(3) NON-MASKABLE INTERRUPT (NMI)

The MSM80C88A has a non-maskable Interrupt (NM1) which is of higher priority than a maskable interrupt request (INTR).

An NM1 request pulse width needs minimum of 2 clock cycles. The NM1 will be serviced at the end of the current instruction or between string manipulations.

(4) MASKABLE INTERRUPT (INTR)

The MSM80C88A provides another interrupt request (INTR) which can be masked by software. INTR is level triggered, so it must be held until interrupt request is acknowledged.

The INTR will be serviced at the end of the current instruction or between string manipulations.

(5) INTERRUPT ACKNOWLEDGE

During the interrupt acknowledge sequence, further interrupts are disabled. The interrupt enable bit is reset by any interrupt, after which the Flag register is automatically pushed onto the stack. During an acknowledge sequence, the CPU emits the lock signal from T2 of first bus cycle to T2 of second bus cycle. At the second bus cycle, a byte is fetched from the external device as a vector which identifies the type of interrupt. This vector is multiplied by four and used as an interrupt pointer address (INTR only).

The Interrupt Return (IRET) instruction includes a Flag pop operation which returns the original interrupt enable bit when it restores the Flag.

(6) HALT

When a Halt instruction is executed, the CPU enter Halt state. An interrupt request or RESET will force the MSM80C88A out of the Halt state.

(7) SYSTEM TIMING-MINIMUM MODE

A bus cycle begins at T1 with an ALE signal. The trailing edge of ALE is used to latch the address. Form T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. From T2 to T4, the address data bus changes the address bus to the data bus.

The read ($\overline{RD}$), write ($\overline{WR}$), and interrupt acknowledge ($\overline{INTA}$) signals caused the addressed device to enable the data bus. These signals become active at the beginning of T2 and inactive at the beginning of T4.

(8) SYSTEM TIMING-MAXIMUM MODE

In maximum mode, the MSM82C88 Bus Controller is added to system. The CPU sends status information to the bus Controller. bus timing signals are generated by the Bus Controller. Bus timing is almost the same as in minimum mode.

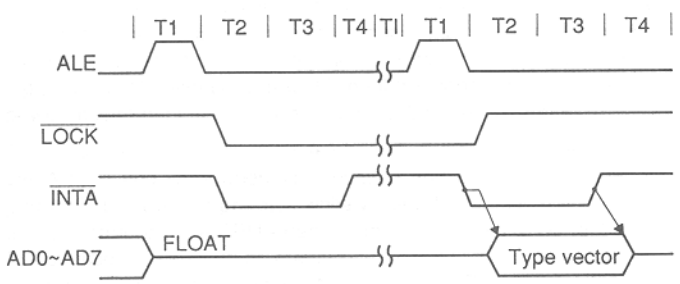


Fig.1-4 Interrupt Acknowledge Sequence

2. DVC ASIC (μPD65658)

2-1. General

The DVC is ASIC having the following functions.

<CPU interface>

- CPU Bus interface

<Memory interface>

- VRAM interface

<Device controller>

- Serial port control (Equality with M8250B)
- Parallel port control
- LCD control

2-2. Block diagram

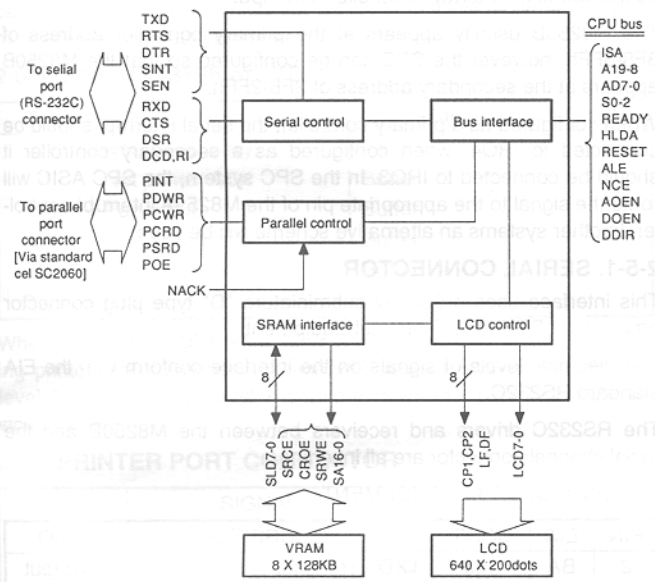


Fig. 2-1. DVC Block diagram

2-3. DVC I/O MAP

ADDRESS (hex)	DEVICE INPUT	DEVICE OUTPUT	NOTE
278	Printer data latch	Printer data latch	※1
279	**	Printer status	※1
27A	Printer control latch	Printer control latch	※1
27B-27F	**	**	
2F8-2FF	M8250B serial controller	M8250B serial controller	※2
378	Printer data latch	Printer data latch	※1
379	**	Printer status	※1
37A	Printer control latch	Printer control latch	※1
37B-37F	**	**	
3B0, 3B2, 3B4, 3B6	MDA 6845 address register	**	※3
3B1, 3B3, 3B5, 3B7	MDA 6845 data register	MDA 6845 data register	※3
3B8	MDA control register	**	※3
3B9	**	**	※3
3BA	MDA status	MDA status	※3
3BB	**	**	※3
3BC	Printer data latch	Printer data latch	※1
3BD	**	Printer status	※1
3BE	Printer control latch	Printer control latch	※1
3BF	**	**	
3D0, 3D2, 3D4, 3D6	CGA 6845 address register	**	※3
3D1, 3D3, 3D5, 3D7	CGA 6845 data register	CGA 6345 data register	※3
3D8	CGA mode control	**	※3
3D9	CGA colour select	**	※3
3DA	**	CGA status register	※3
3DB	Clear light pen latch	**	※3
3DC	Set light pen latch	**	※3
3DD	**	**	※3
3DE	ATT Register	ATT Register	※4
3DF	**	**	※3
3F8-3FF	M8250B serial controller	M8250B serial controller	※2
8400	SPC I/O Key register	**	

** Due to partial decoding of addresses, these addresses should not be used.
Addresses above 3FFh, if accessed, wrap and are mapped onto the range 000-3FFh, Address 8400h does not wrap as expected, this holds the access key to the SPC specific I/O.

※1 The parallel printer port may be configured to appear at its primary address of 378-37Fh, or its secondary address of 278-27Fh, or the MDA printer port address of 3BC-3BFh. The printer port may also be disabled.

※2 The M8250B serial port may be configured to appear at its primary address of 3F8-3FFh, or its secondary address of 2F8-2FFh. The M8250B serial port may also be disabled.

※3 The LCD controller may be configured to appear as an CGA/ATT emulation at address 3D0-3DFh, or a MDA emulation at address 3B0-3BB. The LCD controller may also be disabled.

※4 The ATT register only appears if ATT mode is selected.

2-4. DVC CONTROL I/O MAP

2-4-1. General

The DVC control registers are accessable only when unlocked by writing 44h to location 8400h. When a value other than 44h is written to 8400h, the registers are locked

When the control registers are unlocked the normal I/O at address 000-3FFh does not wrap as expected.

ADDRESS (h)	REGISTER	COMMENT
8400	Key register	Write only
8402	ENABLE	I/O configure
8403	SRPS	SRAM page select
8404	LIND	LCD index
8405	LDTA	LCD data
8406	PMEN	Power Management
FFFF	TEST	For Manufacturing Test, write only

2-4-2. KEY REGISTER (8400h)

To unlock the SPC control I/O a value of 44h must be first written to this register, if any other value is written the SPC control I/O will be relocked.
NOTE. 44h is ASCII "D"

2-4-3. ENABLE

DVC configuration:-

(1) PARALLEL PRINTER PORT

D1	D0	FUNCTION
0	0	PPI is disabled (PPI in low power mode)
0	1	PPI enabled at primary address of 378-37Fh
1	0	PPI enabled at secondary address of 278-27Fh
1	1	PPI enabled at MDA address of 3BC-3BFh

(2) M8250B SERIAL CONTROLLER

D3	D2	FUNCTION
0	0	M8250B is disabled (CLK off)
0	1	M8250B enabled at primary address of 3F8-3FFh
1	0	M8250B enabled at secondary address of 2F8-2FFh
1	1	M8250B is disabled (CLK off)

(3) VIDEO CONTROLLER MODE

D5	D4	FUNCTION
0	0	All video controllers are disabled (CLK off)
0	1	MDA enabled
1	0	CGA enabled
1	1	ATT enabled

D7 & D6 are not implemented and will be read back as '0'.

2-4-4. SRPS

Only used in 8088 MIN & 8088 MAX modes.

D6-0 are used for offset address in 2K pages (64 pages supported).

When DVC is used with 8088 min & 8088 max modes operation this register allows all 128K of memory supported by the DVC to be mapped into CPU address space (allowing character tables and RAM disc to be used).

D7 Disable wrapping.

D7 may be used to turn off wrapping usually associated with the MDA and CGA, when set (D7=1) 32K of DVC memory is directly accessible without paging, starting at the base address associated with the video mode selected (see 2-8. DISPLAY MEMORY MAP).

2-4-5. LIND section

Index address register for LCD configuration.

2-4-6. LDAT

LCD configuration data.

See section 2-7. LCD VIDEO CONTROLLER.

2-4-7. PMEN

This register shadows a register in the SPC ASIC which controls power management.

Bits 7-4, and 2 of this register are not implemented in the DVC and will be read back as '0'.

D3 - LCD power:

When high LCD outputs and the DCC output are enabled.

D1 - Parallel Port Buffer power:

when high Parallel Port outputs are enabled.

D0 - ± 9V supply:
When high Serial Port Buffers have power. i.e.
When low Serial Port output should be tristate.

2-4-8. TEST

This register is used only for device test and is used to multiplex blocks of circuitry to the I/O pins of the device. It is therefore not available for software use. The bits of the register are assigned as follows:

D0 - '1' selects the M8250B block for test
D1 - '1' selects the line buffer RAM for test
D2 - '1' selects the D6845 block for test
D3 - '1' selects the tri-state leakage test
D4 - '1' selects the frame frequency test
D5 - '1' selects the parametric test

The register is reset to '0'. It is assumed that only one test mode will be selected at a time.

2-5. RS232C ASYNCHRONOUS SERIAL PORT

The asynchronous serial port is based on the M8250B, single channel device.

The clock frequency input of the M8250B is 1.8432 MHz (0.1%). This clock is active when the M8250B is enabled. The 1.8432 MHz clock is derived from the CPU clock of 10.00 MHz.

In normal use the BAUD OUT OUTPUT is connected directly to the RCLK input.

An interrupt level is available for uses by the M8250B. The M8250B INT output may be connected to, or disabled from, the interrupt controller by software:-

When the M8250B OUT2 output is driven low then the INT output is connected to an interrupt controller IRQ input.

The M8250B usually appears at the primary controller address of 3F8-3FFh, however the SPC can be configured so that the M8250B appears at the secondary address of 2F8-2FFh.

When configured as a primary controller, the serial interrupt should be connected to IRQ4. when configured as a secondary controller it should be connected to IRQ3. In the SPC system, the SPC ASIC will route the signal to the appropriate pin of the M8259A interrupt controller. In other systems an alternative scheme will be used.

2-5-1. SERIAL CONNECTOR

This interface uses a 25-way subminiature "D" type plug connector emulating a DTE (Data Terminal Equipment)

The electrical levels of signals on the interface conform with the EIA standard RS232C.

The RS232C drivers and receivers between the M8250B and the serial channel connector are all inverting.

(1) CONNECTOR ARRANGEMENT

PIN	EIA	CCITT	DESCRIPTION	I/O
2	BA	103	TXD - Transmit serial Data	Output
3	BB	104	RXD - Receive serial Data	Input
4	CA	105	RTS - Request to send	Output
5	CB	106	CTS - Clear to send	Input
6	CC	107	DSR - Data set ready	Input
7		102	Common return (Ground)	
8	CF	109	DCD - Data Carrier Detect	Input
20	CD	108	DTR - Data Terminal Ready	Output
22	CE	125	RI - Ring Indicator	Input

2-5-2. CLOCK GENERATION

It is not possible to generate 1.8432 MHz from 10.00 MHz using a simple divider, however by dividing using a fixed sequence it is possible to generate 1.8432 MHz with reasonable accuracy (on average).

The divide sequence is:- 5, 6, 5, 6, 5, 6, ...

This gives an average frequency of 1.8421 MHz which is 0.06% slow, but within the 0.1% required.

2-6. PARALLEL PRINTER PORT

The printer port provides a centronics-compatible interface. The timing of signals to the printer is under software control.

The printer port will normally appear at the primary address of 378-37Fh, however it may be configured to appear at the secondary address of 278-27Fh or MDA address of 3BC-3BFh.

This port is implemented using latches and buffers external to the DVC ASIC. This is to save pins and to ensure correct buffering for the interface.

2-6-1. DATA LATCH (378h or 37Ch)

The data latch is 8 bit Output/Input.

The contents of the data latch are undefined following a power-up or system reset. Data is read back from a latch inside the DVC.

2-6-2. CONTROL LATCH (37Ah or 37Eh)

BIT	Output/Input
D7-5	No effect
D4	Enable interrupt on ACK
D3	Select printer
D2	Not reset printer
D1	Select auto feed
D0	Data strobe

All bits of the printer control latch are cleared by reset.

The timing requirements on centronics printers generally specify that the data must be present at least 1μS before the strobe is made active, and must remain valid for at least 1μS after the strobe. The duration of the strobe must be between 1μS and 500μS. The status can be inspected as soon as the strobe is inactive in order to determine when more data can be sent.

2-6-3. STATUS (379h or 37Dh)

Bit	Input	Connector input Buffer type
D7	Not printer busy	Inverter
D6	Not printer ACK	Buffer
D5	Paper out	Buffer
D4	Printer selected	Buffer
D3	Not printer error	Buffer
D2-0	Undefined	

When interrupt on ACK is enabled in the printer control latch, incoming printer Acknowledge condition will cause a system interrupt on level 7. Note interrupt level 7 is also available for use on the expansion bus.

2-6-4 PRINTER PORT CONNECTOR

2PIN	SIGNAL	TYPE
1	Not Data Strobe	Output/(Input)
2	Data 0	Output
3	Data 1	Output
4	Data 2	Output
5	Data 3	Output
6	Data 4	Output
7	Data 5	Output
8	Data 6	Output
9	Data 7	Output
10	Not printer ACK	Input
11	Printer busy	Input
12	Paper out	Input
13	Not printer select	Input
14	Not select auto feed	Output/(Input)
15	Not printer error	Input
16	Not printer reset	Output/(Input)
17	Select printer	Output/(Input)
18-25	Ground (0 volts)	

(Input) These signals are usually driven by open collector drivers, however in this application where power saving is vital they will be output only, should an external device drive one of these outputs it will be protected by a suitable series resistor (to be decided).

2-6-5. IMPLEMENTATION OF PARALLEL PORT HARDWARE

The parallel port hardware implementation uses external buffers and latches in order to reduce the external pin-count and to ensure the correct drive levels and strengths.

(1) **Data Latch**-should be implemented as an octal edge triggered latch, the strobe for the latch is pdw. The read-back path for this latch is from a register inside the DVC.

(2) **Control Latch**-should be implemented as an edge triggered latch, strobed by PCW. Bit 4 of this register is implemented inside the DVC, and the NACK signal from the interface should be connected to the DVC and this is used to drive the parallel port interrupt line. PCR is the read strobe for this port.

(3) **Status Port**-The read strobe (output enable for a buffer) for this port is PSR.

All the parallel port strobes are active low. Data bus connections are either direct to the CPU AD bus, or via a buffering scheme such as the one used for ISA (PC) bus mode.

2-7 LCD VIDEO CONTROLLER

This section should be read in conjunction with D6845 VIDEO CONTROLLER.

To allow the use of smaller LCDs than 640 x 200 or 640 x 400 various configuration registers have been provided, these configuration registers are only accessible when the SPC control I/O has been unlocked, via the register at 8400h.

2-7-1 STATUS CONTROL

Status lines are displayed at the end of active MDA, CGA or ATT display. The status display can be any length programmed. The length of the display is derived from the difference between the vertical total register and vertical displayed register (DSTV-DSV)

The status information starts at the location in SRAM indicated by SPC system configuration register DSST, the status information has same format as CGA graphics 640 x 200 (mode 2), but continuously in memory.

2-7-2 LCD CONTROL REGISTERS

The following registers are available when the SPC configuration I/O has been unlocked at address 8404 & 8405.

8404h is the index register (4 bit)

8405h is the Data register

INDEX	REGISTER	COMMENT
0	DTH	Horizontal display + border in characters.
1	DSH	Horizontal display size in characters.
2	MALT	Number of line per LCD DF signal alternation.
3	TPVS	Top Panel Vertical Size
4	DSTV	Vertical display + Status in pixels.
5	DSV	Vertical display in pixels.
6	DSOL	LCD offset address.
7	DSOU	(in characters)
8	MCR0	Mode Control Register 0
9	MCR1	Mode Control Register 1
10	DSST	Display status start address/512.
11	DSCT	Character table start address/512.
12	DSGS1	Gray scale set GS1.
13	DSGS2	Gray scale set GS2.
14	DCC	Contrast voltage.

(1) DTH
This 8 bit register defines the horizonal display width in characters of the LCD and the number of character periods which the LCD controller waits before starting the next line.

(2) DSH
This 8 bit register defines the horizontal display width of the LCD in characters.

(3) MALT
This 8 bit register defines the number of line periods between an alternation of the phase of the LCD DF alternating signal. This can be used to enhance the sharpness of some LCD displays.

(4) TPVC
This 8 bit register defines the size of the top display. This is used in the situation where two LCD panels of unequal size are used to form the display.

(5) DSTV
This 8 bit register defines the vertical total in pixels of the LCD display, this is made of two parts, the display height in pixels and the status height in pixels.

(6) DSV
This 8 bit register defines the vertical display height in pixels.

(7) DSOU + DSOL
This 16 bit register defines the number of memory locations to the top left corner of the LCD, from the address defined in D6845 R12 & R13.

(8) EXAMPLES OF HOW THESE REGISTERS ARE USED:
Single Display: 200 Line LCD, 4 Status lines to be displayed
DSTV=200
DSV=196
TPVC=X i.e. it is ignored
Double Display: 2 200 Line LCD Panels, 4 Status line to be displayed
DSTV=200
DSV=196
TPVC=200
Double Display: Top LCD 200 line, bottom LCD 100 lines, 10 status lines
DSTV=200
DSV=90
TPVC=200

(9) MCR0

Mode control register 0

BIT	NAME	COMMENT
D7	THN	If = 1 in 40*25 alpha, each PEL is 1 pixel wide not 2
D6	LLB	If = 1 blank last line if IBM standard character font
D5	PWD1	Defines the LCD interface data width as 1, 2, 4 or 8 bits
D4	PWD0	
D3	INV	If = 1 all LCD data is inverted
D2	ULI	If = 0 underline is on scan 7, if = 1 scan 8
D1	CWD1	Defines horizontal size of character, 6, 7, 8 or 9 PEL, only applicable in alpha modes.
D0	CWD0	

PEL = Picture Element, a PEL may be 1 or more pixels in size.
CWD1 & CWD0 when set to 9, the ninth PEL is always background colour.
LLB - Note the following:
BLANK DETECTION ALGORITHM.
In order to save power, the DVC does not do any unecessary accesses to external SRAM in order to fetch data for the video display. In Alpha modes a line buffer is used to store character and attribute data. During the first scan of a character row this buffer is filled, during subsequent scans it is only necessary to fetch font data. However, if the character font information to be fetched is known to have no bits set - i.e. it is a space or the last row of most characters - then no font data is fetched either. The characters which will cause the DVC to fetch font information on the last row are:

05h - Box character
08h - Box character
5Fh - Underline
Any character with a character code > B0h

This feature can be switched off using bit 6 of MCR0, this allows the use of non-standard character sets.
Note that the blank character (20h) will never be fetched from the font RAM, irrespective of the state of LLB.

(10) MCR1

Mode control register 1

BIT	NAME	COMMENT
D4	LKMDA	Lock MDA. Fixes character size to 8 rows in MDA mode
D3	DLC	If = 1 LCD screen is made using two LCD panels dimensions of which are defined using DSHL, DSHU, DSV.
D2	DUP	If = 1 all pixels are duplicated.
D1	SHF	If = 1 scans are quadrupled.
D0	SHT	If = 1 scans are duplicated.

SHT & SHF

D1	D0	Comment
0	0	Each scan is only displayed once.
0	1	Each scan is displayed twice
1	x	Each scan is displayed four times.

(11) DSST
Status Start address, this defines from which 512 byte boundary in SRAM the status information is to be found.
Status information has same format as CGA graphics mode 2. The display will be as per CGA graphics mode 2, i.e. it will not be affected by MCR1.
N.B. For status to work correctly where there are two LCD panels of unequal size being used, then either the top panel should be smaller than the lower one, or only eight bit characters should be used, with MCR1 set to 0h.

(12) DSCT
Start Character Table, this register defines from which 512 byte boundary in SRAM the character table starts.

(13) DSGS1
Each bit indicates if a PEL of GS1 is on (=1) or off (=0) during this frame.
D0 = 1 PEL of GS1 is on during frame 1.
D1 = 1 PEL of GS1 is on during frame 2.
etc...
D7 = 1 PEL of GS1 is on during frame 8.

(14) DSGS2
Each bit indicates if a PEL of GS2 is on (=1) or off (=0) during this frame.
D0 = 1 PEL of GS2 is on during frame 1.
D1 = 1 PEL of GS2 is on during frame 2.
etc...
D7 = 1 PEL of GS2 is on during frame 8.

(15) DCC
See section 2-10. CONTRAST CONTROLLER

2-7-3. ATT MODE

The LCD display used for ATT mode is made of two identical panels, the values used to define the display size are for any panel.

2-8. DISPLAY MEMORY MAP

The following table shows how the Display RAM for the various main display modes is mapped onto CPU memory address space when the Display Controller is enabled:-

CPU Address	MDA Map	CGA Map	ATT Map
BFFFFh ≀ BC000h		Repeat of CGA 16K block	ATT Modes 32K
BBFFFh ≀ B8000h		CGA Modes 16K block	
B7FFFh ≀ ≀ B1000h	7 repeats of MDA 4K block (28K)		
B0FFFh B0000h	MDA Mode 4K		

The above mapping is only valid when the DVC ASIC is in either 8088 MIN or 8088 MAX modes, when in 8088 MAX + Memory Map mapping depends on how memory mapping registers have been configured.

2-8-1. TEXT DISPLAYS

Each character position displayed in text modes is represented by a pair of contiguous bytes in display RAM. The even addressed byte of each pair stores a character code which determines which of 256 different characters is to be displayed, while the odd byte stores a character attribute which determines how the character is to be displayed in terms of colour, reverse video, underlining, blinking etc.

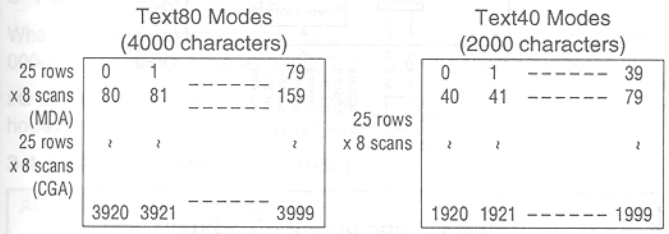
(1) TEXT DISPLAY RAM MAPPING

The following tables show how the character codes and attribute bytes stored in RAM relate to the display for the various text modes.

Text Mode Memory Organization

Memory Address for CRTC start address = 0			Character No & Byte Type	Comment
MDA Text80	CGA Text80	CGA Text40		
B0000h B0001h	B8000h B8001h	B8000h B8001h	0 Code 0 Attr	1st character position (top LH corner)
B0002h B0003h	B8002h B8003h	B8002h B8003h	1 Code 1 Attr	2nd character position (1st row 2nd column)
≀	≀	≀	≀	
		B87CEh B87CFh	1999 Code 1999 Attr	Text40 last position (25th row 40th column)
			≀	
B0F9Eh B0F9Fh	B8F9Eh B8F9Fh		3999 Code 3999 Attr	Text80 last position (25th row 80th column)

Text Mode Display Organization



The first displayed character in the top left corner of the screen (row 0, column 0) is that whose modulo 16K character code byte address ≈ 2 is programmed into the M6845 CRTC's 14 bit Start Address register; the above tables assume a start of 0000h.

The memory space normally available for displaying MDA text is 4K bytes (2K characters).

The memory space available for displaying CGA text is 16K bytes (8K characters).

2-8-2. CGA GRAPHICS

In both CGA Graphic640 and Graphic320 modes the CRTC is programmed for 100 rows of characters of 2 scans each, and a character represents two bytes stored in RAM, one for the even scan and one for the odd scan. (Graphic160 mode, a very low resolution 160†100 dots in 16 colours, is not strictly graphics at all, but just a special application of Text80 mode with only two scans per row, which uses some half-block characters from the font to give two 'dots' per character. This mode will not be discussed further).

The bytes for the even scans 0, 2, 4, – – – – –, 196, 198 are stored in the first half of 16K RAM starting at B8000h, and those for the odd scans 1, 3, 5, – – – – – 197, 199 are stored in the second half starting at BA000h.

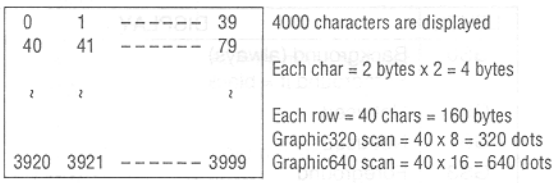
(1) GRAPHICS DISPLAY RAM MAPPING

The following tables show how the bytes stored in RAM relate to the display for the various graphics modes.

CGA Graphic320 & Graphic640 Memory Organization

RAM Addr for CRTC Start = 0	Char No	Scan No	Comment
		(Odd)	
B8000h	0	0	1st position (top LH corner)
B8001h	1	0	2nd position (1st row 2nd column)
≀	≀	≀	
B9F3Fh	7999	198	Last position (100th row 80th column)
		(Even)	
BA000h	0	1	1st position 2nd scan
BA001h	1	1	2nd position 2nd scan
≀	≀	≀	
BBF3Fh	7999	199	last position 2nd scan, bottom RH corner (ie 200th displayed scan)

CGA Graphics Display Organization



The first displayed character in the top left corner of the screen (row 0, column 0) is that whose modulo 16K even byte address ≈ 2 is programmed into the M6845 CRTC's 14 bit Start Address register; the above tables assume a start address of 0000h. It follows that a Graphic320 display may only be offset horizontally in 8 dot increments, and a Graphic640 display in 16 dot increments. Both modes may only be offset vertically in 2 scan increments.

The memory space available for displaying CGA graphics is 16K bytes (4K characters).

2-9. LCD COLOUR MAP

This section should be read in conjunction with MDA VIDEO CONTROLLER and CGA VIDEO CONTROLLER sections.

2-9-1. LCD GRAY SCALE

The LCD supports 4 gray levels these are, GS0 (OFF), GS1, GS2 & GS3 (ON). Grey levels are made by turning pixels on and off on an eight frame cycle.

GS0, is always off.
GS1, DSGS1 bits D0-7 define which frames in eight the PEL is on.
GS2, DSGS2 bits D0-7 define which frames in eight the PEL is on.
GS3, Is always on.

DSGS1 & DSGS2 are LCD control registers.

2-9-2. MDA MAPPING

LEVEL	DISPLAY
GS0	Normal white on black, background Inverse black on white, foreground
GS1	Normal white on black, foreground Inverse black on white, background
GS3	Normal white on black highlighted, foreground Inverse black on white highlighted, background

2-9-3. CGA MAPPING

(1) ALPHA MODES

The two alpha modes 80 x 25 (high resolution) & 40 x 25 (low resolution) are mapped as follows:-

LEVEL	DISPLAY
GS0	Black background or foreground
GS1	Coloured background Coloured foreground if = background (except black)
GS2	Coloured foreground
GS3	Intensified foreground

(2) GRAPHICS MODES

① GRAPHICS MODE 1 (320 x 200)

Three palettes are mapped as follows:-

LEVEL	DISPLAY
GS0	Bit 1 = 0, Bit 0 = 0. Background
GS1	Bit 1 = 0, Bit 0 = 1. or Background if = colour.
GS2	Bit 1 = 1, Bit 0 = 0. or Background if = colour.
GS3	Bit 1 = 1, Bit 0 = 1. or Background if = colour.

② GRAPHICS MODE 2 (640 x 200)

This is a monochrome display the mapping is as follows:-

LEVEL	DISPLAY
GS0	Background (always) Foreground if = black
GS1	Not used
GS2	Not used
GS3	Foreground

2-9-4. ATT MODE

Mapping is the same as CGA, the additional ATT mode is same as CGA graphics mode 2.

2-10. CONTRAST CONTROLLER

2-10-1. INTRODUCTION

This 8bit register controls the duty cycle of the CDC output. The CDC output is used to control the contrast voltage of an LCD display (-VEE).

2-10-2. CONTRAST CONTROLLER I/O

SIGNAL	TYPE	DESCRIPTION
D6-0	Input	Data
NRST	Input	Reset
CCLK	Input	Clock 10MHz
CDC	Output	Variable mark space 0/128 to 128/128 at 300Hz.

(1) DATA (D7-0)

D7-0 are the data inputs D0 correspond to bit 0 of the register.

(2) CLOCKS (CLK & CDC)

The CDC output is derived from the 10MHz system clock, this is first divided by 256, then by 128 to produce the CDC output, the duty cycle of the CDC output will depend on the value programmed in the the DCC register.

2-10-3. CONTRAST CONTROL REGISTER DCC

This eight bit register defines the contrast duty cycle.

If DCC = 00h then CDC will be low (continuous).
If 80h > DCC > 00h CDC duty cycle is dependent on DCC value.
If DCC > = 80h then CDC will be high (continuous).

3. SPC ASIC (TC146G68)

3-1. General

The SPC is ASIC having the following functions.

<CPU interface>

- Generation of various kinds of interruption
- CPU bus control
- Expansion bas control

<Memory interface>

- Memory mapper
- Local memory control
- DMA controller

<Device control>

- DVC control
- Keyboard control
- Sound control
- Power control

3-2. Block diagram

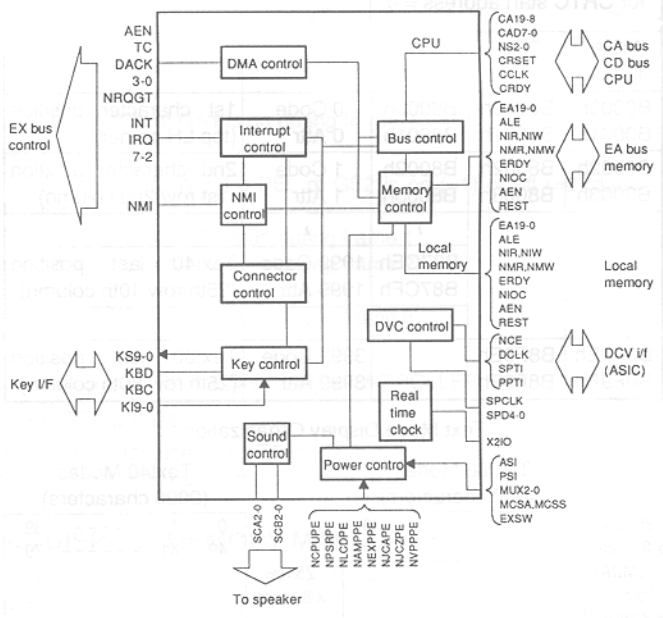


Fig 3-1. SPC BLOCK DIAGRAM

3-3. SPC I/O MAP

ADDRESS hex	DEVICE INPUT	DEVICE OUTPUT
000-00F	M8237A DMA controller	M8237A DMA controller
010-01F	**	**
020-021	M8259A Interrupt controller	M8259A Interrupt controller
022-03F	**	**
040-043	M8253 PIT controller	M8253 PIT controller
044-05F	**	**
060	**	M8255 port A
061	M8255 port B	M8255 port B
062	**	M8255 port C
063-07F	**	**
080	**	**
081	DMA page register 2	**
082	DMA page register 3	**
083	DMA page register 0 & 1	**
084-09F	**	**
0A0	NMI mask control bit	**
8400	SPC I/O Key register	**

** Due to partial decoding of addresses, these addresses should not be used.
Addresses above 3FFh, if accessed, wrap and are mapped on to the range 000-3FFh, Address 8400h does not wrap as expected, this holds the access key to the SPC specific I/O.
Accesses to devices within the SPC or DVC ASICs do not appear on the expansion bus, however NMI mask register does.

3-3-1 MAPPING REGISTER I/O

The 64 page registers are accessed through three consecutive addresses in I/O space. An SPC configuration register selects the base I/O address to be used for page register access.

Page registers are accessed as follows:-
I/O ADDRESS, REGISTER, DESCRIPTION

BASE + 0	PRN5-0	Page register select
BASE + 1	PRN5-0	Page register select
BASE + 2	MA-0	Mapping address lsb
BASE + 3	MA15-8	Mapping address msb

BASE+0 and base+1 are both mapped to the same register.
Usual addresses for Mapping registers are :-
208h, 218h, 228h, 238, etc..., 2E8 & 2F8.

Care must be taken when selecting an I/O address for the mapping registers that it does not conflict with other devices or uses reserved I/O locations.

3-4 SPC CONTROL I/O MAP

When the SPC control I/O is unlocked the normal I/O at address 000-3FFh does not wrap as expected within its address range.

I/O at these addresses can only be accessed if it has been unlocked, however address 8400h is always accessable.

3-4-1 SPC CONTROL I/O TABLE

ADDRESS (h)	REGISTER	COMMENT
8400	Key register	01h read back when unlocked
8401	LIMIO	Memory map I/O base
8402	ENABLE	I/O configure
8403	SRPS	SRAM page select 1
8404	LIND	LCD Index register 1
8405	LDAT	LCD data 1
8406	PCNTR	Power control register
8407	CCNTR	Clock control register
8408	CPCG	CPU clock speed
8409	ROMP	JEIDA programming control
840A	PASR	M8255 status latch
840B	PASR	
840C	NMI08	SPC NMI vectors
840D	NMI09	
840E	NMI0A	
840f	NMI0B	
8410	SISR	SPC interrupt source register
8411	SISE	SPC interrupt enable
8412	PSIR	Power supply int. register
8413	PSIE	Power supply int. enable
8414	PSIS	Power supply status
8415	ISIR	Internal service int. register
8416	ISIE	Internal service int. enable
8417	MIR	Memory int. register
8418	MIR	Memory int. enable
8419	MIS	Memory status
841A	RSTR	CPU reset source register
841B	KSTR	LCD Status Register
841C-84 1F	**	
8420	ATR0	Address trap
8421	ATR1	
8422	ATR2,	
8423	**	
8424	MAV0	Memory access violation
8425	MAV1	
8426	MAV2,	
8427	**	
8428	ACR lsb	Activity register
8429	ACR	
842A	ACR msb	
842B	ACM	Activity mask register
842C	SWG0	Sound channel 0
842D	SWG0	
842E	SWG1	Sound channel 1
842F	SWG1	
8430	SCR-ISCR	Keyboard
8431	ARR	Keyboard auto repeat
8432	PDR lsb	Keyboard power down
8433	PDR msb	
8434	WSR0	Keyboard warm start
8435	WSR1	
8436	WSR2	
8437	SKWR	Single key wake-up
8438-F	**	
8440	TCR lsb	DTC Tick Count Register
8441	TCR	
8442	TCR	
8443	TCR msb	
8444	TKI lsb	DTC Tick interrupt register
8445	TKI	
8446	TKI	
8447	TKI msb	
8448	TMI lsb	DTC Timer interrupt register
8449	TMI	
844A	TMI	
844B	TMI msb	
844C-F	**	
8450	RTR lsb	RTC counter register
8451	RTR	

ADDRESS (h)	REGISTER	COMMENT
8452	RTR	
8453	RTR	
8454	RTR msb	
8455-57	**	
8458	RTI lsb	RTC interrupt register
8459	RTI	
845A	RTI	
845B	RTI	
845C	RTI msb	
845D	TR	DTC timer control register
845E-F	**	

1 These registers are not in the SPC ASIC.

3-4-2 KEY REGISTER (8400h)

To unlock the SPC control I/O a value of 44h must be written to this register, if any other value is written the SPC control I/O will be locked.

If the SPC control I/O is locked a value of 00 will be read from this register.
If the SPC control I/O is unlocked a value of 01 will be read from this register.

3-4-3 LIMIO (8401h)

This register defines the BASE address of the memory mapping registers (LIM) in I/O space.

D7-0 correspond to A9-A2 of I/O address.

3-4-4 ENABLE (8402h)

(1) PARALLEL PRINTER PORT

D1	D0	FUNCTION
0	0	PPI is disabled
0	1	PPI enabled at primary address of 378-37Fh
1	0	PPI enabled at secondry address of 278-27Fh
1	1	PPI enabled at MDA address of 3BC-3BFh

(2) M8250B SERIAL CONTROLLER

D3	D2	FUNCTION
0	0	M8250B is disabled
0	1	M8250B enabled at primary address of 3F8-3FFh
1	0	M8250B enabled at primary address of 2F8-2FFh
1	1	M8250B is disabled

(3) VIDEO CONTROLLER MODE

D5	D4	FUNCTION
0	0	All video controllers are disabled
0	1	MDA enabled
1	0	CGA enabled
1	1	ATT enabled

Bits D6 and D7 are undefined, they are read back as 0.

3-4-5 SRPS (8403h)

Only used in 8088 MIN & 8088 MAX modes.

Only D6-0 are used for offset address.

When the DVC is used with 8088 min & 8088 max modes operation this register allows all 128K of memory supported by the DVC to be mapped into CPU address space.

3-4-6 LIND (8404h)

Address register for LCD configuration.

See DVC ASIC specification section LCD VIDEO CONTROLLER.

3-4-7 LDAT (8405h)

LCD configuration data.

See DVC ASIC specification section LCD VIDEO CONTROLLER.

3-4-8 PASR REGISTERS (840Ah, 840Bh)

These two registers replace switches usually found on a PC mainboard, see M8255 section.

All other registers are defined in their relevant sections.

3-5. SPC INTERRUPTS

All interrupts in the SPC are listed below:

INT	TYPE	SOURCE	CLEARED
IRQ0	INT	PIT OUT0	M8259a
IRO1	INT	Keyboard	M8259a
IRO2	INT	Expansion bus	M8259a
IRO3	INT	Expansion bus	M8259a
IRO4	INT	Exp bus/Serial control	M8259a
IRO5	INT	Expansion bus	M8259a
IRO6	INT	Expansion bus	M8259a
IRO7	INT	Exp bus/Parallel port	M8259a
IOCHK	NMI	I/O check on exp bus	Write M8255 PB5
KINT	NMI	Matrix keyboard	Read SCR
EXPI	NMI	Expansion unit switch	Read MIR
AABL1	NMI	AA battery level	Read PSIR
AABL0	NMI	AA battery level	Read PSIR
LIBL	NMI	Lithium cell level	Read PSIR
EXBL1	NMI	Expansion battery level	Read PSIR
EXBL0	NMI	Expansion battery level	Read PSIR
MABL	NMI	Memory card A batt level	Read PSIR
MBBL	NMI	Memory card B batt level	Read PSIR
ACPWR	NMI	AC Power level	Read PSIR
RTCINT	NMI	Real Time Clock	Read RTI
TICI	NMI	DTC tick timer	Read TKI
TIMI	NMI	DTC timer	Read TMI
SPCA	NMI	Activity detector	Read ACM
PATR	NMI	Address trap	Read ATR2
KBPD	NMI	Keyboard power down reg	Read SCR
MCWPA	NMI	Memory card A write protect	Read MTR
MCWPB	NMI	Memory card B write protect	Read MTR
MCDA	NMI	Memory card A detect	Read MTR
MCDB	NMI	Memory card B detect	Read MTR
MAVI	NMI	Memory access violation	Read MAV2
WINT	NMI	Matrix Keyboard Wake-Up	Read SISR
MCSA	NMI	Memory card A switch	Read MIR
MCSB	NMI	Memory card B switch	Read MIR
EXSW	NMI	Expansion Unit switch	Read MIR

3-6. M8259A INTERRUPT CONTROLLER

3-6-1 GENERAL DISCUSSION

Addressed at 020-03Fh.
Eight levels of hardware interrupt are supported by the M8259A interrupt controller.
The M8259A interrupt controller has A0 connected conventionally so that command codes appear in the expected order as in the M8259A specification. The M8259A is at address 020-021h.
In normal use SP/EN input is tied high indicating that the device is hardware un-buffered and designated as a master.

3-6-2 INTERRUPT LEVEL

The interrupt levels are assigned as follows:-

Level 0	M8253 PIT OUT0
Level 1	Keyboard receive logic
Level 2	Available on expansion bus.
Level 3	Available on expansion bus. (serial controller when enabled at secondary address)
Level 4	Available on expansion bus. (serial controller when enabled at primary address)
Level 5	Available on expansion bus.
Level 6	Available on expansion bus.
Level 7	Available on expansion bus. (Parallel Printer Port when enabled)

3-6-3 M8259A INITIALISTATION

Following a system reset, system initialisation software should set the M8259A as follows:-

8086 system
Single (not cascade)
Normally fully nested
Edge triggered
Buffered mode
Normal EOI
Fixed priority-level 0 highest, level 7 lowest.

3-7 NMI control

3-7-1 GENERAL DISCUSSION

There are two sources of NMI, those normally associated with PC systems and those generated by SPC specific features (ie SPC matrix keyboard KINT).

3-7-2 SYSTEM NMI

INTERRUPT SOURCE
NMI I/O Check from expansion bus

Note. No system memory is parity checked, nor is there a co-processor fitted (8087).
The expansion bus I/O Check input is enabled or disabled via M8255 PB5 (port B bit 5).
The IOCHK NMI (from the expansion bus) can be masked under software control (0A0h bit D7, write only).

3-7-3 SYSTEM NMI MASK

Addressed at 0A0h

BIT	Output use
D7	Enable System NMI
D6-0	No effect

Following a reset, NMI is disabled.
CPU accesses to this register will also appear on the expansion bus.

3-7-4 SPC SPECIFIC NMI

The SPC has a set of special interrupt sources, these are from SPC specific blocks, such as power management, matrix keyboard etc..
When an SPC specific interrupt is acknowledged the NMi vector read by the CPU from memory addresses 00008-0000Bh is intercepted, and data held in system configuration registers NMI08-NMI0B is substituted.
If the NMI is non SPC specific (I/O check) the NMI vector is read from memory 00008-0000Bh as expected.
SPC specific interrupts may be read back from SPC status register SISR as follows:-

INTERRUPT	SOURCE	REGISTER
		SISR D7
		SISR D6
WINT	Matrix keyboard	SISR D5
KINT	Matrix keyboard	SISR D4
PSINT	Power status	SISR D3
ISINT	Internal service	SISR D2
MCINT	JEIDA memory cards	SISR D1
MAVI	Memory access violation	SISR D0

This register is read only, reading the register will clear bits D1, 4 & 5.
All interrupts can be enabled/disabled by setting/clearing the corresponding bits if SISE register.
Bit D6, D7 are always read back as 0.

3-7-5 PSINT

The source of the PSINT can be read from the PSIR register an follows:

Interrupt	source	register
AABL1	AA batteries low	PSIR D7
AABL0	AA batteries flat	PSIR D6
LIBL	Lithium battery flat	PSIR D5
EXBL1	Expansion batteries low	PSIR D4
EXBL0	Expansion batteries flat	PSIR D3
MABL	JEIDA card A batteries low	PSIR D2
MBBL	JEIDA card B batteries low	PSIR D0
ACPWR	External power low	PSIR D0

This register is read only, reading the register will clear it.
All interrupts can be enabled/disabled by setting/clearing the corresponding bit in PSIE
The status of the power sources can be read at any time from PSIS.
PSIS is updated once per millisecond.

3-8. MEMORY MAP

Memory space (1 M byte) is divided into 64 16K page each page having an associated mapping register, all mapping registers are programmable.
Both CPU and DMA cycles, will also be protected during DMA cycles.

3-8-1 MEMORY MAP REGISTERS

Table of memory mapping registers and their associated address range.

No	Address to		COMMENTS
0	00000	03FFF,	
1	04000	07FFF,	
2	08000	0BFFF	
3	0C000	0FFFF	
4	10000	13FFF	
5	14000	17FFF	
6	18000	1BFFF	
7	1C000	1FFFF	
8	20000	23FFF	
9	24000	27FFF	
10	28000	2BFFF	
11	2C000	2FFFF	
12	30000	33FFF	
13	34000	37FFF	
14	38000	3BFFF	
15	3C000	3FFFF	256K boundary
16	40000	43FFF	
17	44000	47FFF	
18	48000	4BFFF	
19	4C000	4FFFF	
20	50000	53FFF	
21	54000	57FFF	

No	Address to		COMMENTS
22	58000	5BFFF	
23	5C000	5FFFF	
24	60000	63FFF	
25	64000	67FFF	
26	68000	6BFFF	
27	6C000	6FFFF	
28	70000	73FFF	
29	74000	77FFF	
30	78000	7BFFF	
31	7C000	7FFFF	512K boundary
32	80000	83FFF	
33	84000	87FFF	
34	88000	8BFFF	
35	8C000	8FFFF	
36	90000	93FFF	
37	94000	97FFF	
38	98000	9BFFF	
39	9C000	9FFFF	640K boundary
40	A0000	A3FFF	
41	A4000	A7FFF	
42	A8000	ABFFF	
43	AC000	AFFFF	
44	B0000	B3FFF	Used by MDA
45	B4000	B7FFF	Used by MDA
46	B8000	BBFFF	Used by MDA
47	BC000	BFFFF	Used by MDA
48	CC000	C3FFF	
49	C4000	C7FFF	
50	C8000	CBFFF	
51	CC000	CFFFF	
52	C0000	D3FFF	
53	D4000	D7FFF	
54	D8000	DBFFF	
55	DC000	DFFFF	
56	E0000	E3FFF	
57	E4000	E7FFF	
58	E8000	EBFFF	
59	EC000	EFFFF	
60	F0000	F3FFF	60-63 Used by BIOS
61	F4000	F7FFF	
62	F8000	FBFFF	
63	FC000	FFFFF	

Following a system reset the memory mapping registers will be disabled and all memory accesses will be mapped to device 0 (OTPROM0) page 4095. While disabled the mapping registers can be accessed by the CPU and software should set up all registers even if some are not used. When the msb of register 63 has been written the mapping registers will be enabled.

3-8-2 MAPPING REGISTER FORMAT

(1) MAPPING REGISTER I/O

The 64 page registers are accessed through three consecutive addresses in I/O space. An SPC configuration register selects the base I/O address to be used for page register access.

Page registers are accessed aa follows:-

I/O ADDRESS	REGISTER	DESCRIPTION
BASE + 0	PRN5-0	Page register select
BASE + 1	PRN5-0	Page register select
BASE + 2	M7-0	Page register data lsb
BASE + 3	M15-8	Page register data msb

BASE+0 and base+1 are both mapped to the same register.
After power-up all page registers are undefined.

(2) MAPPING REGISTER FORMAT

Each mapping register is 16 bits wide (M15-0), the bits are allocated as follows:-

BIT FUNCTION
MA15-12 Device select
MA11-0 Address map and Read only Enable bits

① DEVICE SELECT

MA15-12	DEVICE	COMMENT
0	OPTROM0	
1	OPTROM1	
2	ROM0	
3	ROM1	
4	PSRAM0	
5	PSRAM1	
6	PSRAM2	Optional (may not be fitted)
7	PSRAM3	Optional (may not be fitted)
8	JEIDA A R/W	Read/Write
9	JEIDA A R	Read only
A	JEIDA B R/W	Read/Write
B	JEIDA B R	Read only
C	SRAM R/W	Read/Write
D	SRAM R	Read only
E	Expansion Bus	
F		No memory device selected

② PAGE SELECT

Read only devices (OTPROM0, OTPROM1, ROM0 & ROM1) and JEIDA cards
Up to 4096 page (12 bit MA11-0) of 16K byte can be selected (64M byte).
Devices with less than 4096 page will wrap.
The OTPROMs and ROMs are externally limited to 1M byte.

③ PSRAM

Up to 256 pages (MA7-0) of 16K byte can be selected (4096K byte),this is externally limited to 1M byte.
Each of the 16K page is further divided into 4K segments, each 4K segment can be made either Read/Write (bit = 0) or Read Only (bit = 1), 4 bits usually used for paging (MA11-8) are allocated for this function.

BIT	BIT=0	BIT=1
MA8	4K segment 0 is R/W	4K segment 0 is Read only
MA9	4K segment 1 is R/W	4K segment 1 is Read only
MA10	4K segment 2 is R/W	4K segment 2 is Read only
MA11	4K segment 3 is R/W	4K segment 3 is Read only

If a PSRAM segment set Read only is written, a memory access violation interrupt is generated (NMI), and the write will fail.

④ SRAM

Up to 16 page (MA3-0) of 16K byte can be selected (256K BYTE).
For device select C, each of the 16K pages is divided into 2K segments, each 2K segment being made either Read/Write (bit = 0) or Read Only (bit = 1), 8 bits usually used for paging (MA11-MA4) are allocated for this function.

BIT	BIT=0	BIT=1
MA4	2K segment 0 is R/W	2K segment 0 is Read only
MA5	2K segment 1 is R/W	2K segment 1 is Read only
MA6	2K segment 2 is R/W	2K segment 2 is Read only
MA7	2K segment 3 is R/W	2K segment 3 is Read only
MA8	2K segment 4 is R/W	2K segment 4 is Read only
MA9	2K segment 5 is R/W	2K segment 5 is Read only
MA10	2K segment 6 is R/W	2K segment 6 is Read only
MA11	2K segment 7 is R/W	2K segment 7 is Read only

If SRAM device select is D then whole 16K page is Read only irrespective of the state of MA11-MA4
If a SRAM page or segment which is set Read only is written, a memory access violation interrupt is generated (NMI), and the write will fail.

3-9. DIP KEYBOARD INTERFACE (DKI)

3-9-1 GENERAL DISCUSSION

The keyboard interface will produce a scan-code based on an 11*11 key switch matrix, allowing for a maximum of 121 keys. The interface will produce a scan-code between 0 and 78h (0-120). A flag indicating whether the scan-code was generated on a press or a release will be provided.

A key action will generate a keyboard interrupt (KINT). The processor will read the scan-code Register (SCR) to get the scan-code for that key action. The top bit will be set to indicate a key release. Only one interrupt for each press and each release will be generated. It is important that if an interrupt is sent to the processor, the scan-code of the key that generated that interrupt is read by the processor. Once a key press action has been read by the processor, and if no changes occur within a number of scans (dictated by the auto-repeat register (ARR)) then interrupts will be generated repeatedly each scan.

The keyboard controller will scan the 11*11 matrix, junction by junction. A counter will follow the scan and will thus be holding the current scan-code. This scan-code will be loaded into the SCR when that key state changes. The current state of the keyboard could be stored in a 121 bit shift register. Each bit would represent one key on the keyboard. Each register bit would store the value of the last key used (press or release). When the register and keyboard have different values, a toggle has occurred and a key action is detected.

A set of three registers (Warm Start Registers-WSR) will hold a set of scan-codes. When each of the three scan-codes are pressed on any one scan, a warm start will be generated. Warm start may be disabled by setting the WSRs to a value greater than 121.

The single key wake-up register (SKWR) will hold a scan-code in the 7 lsbs. When this scan-code is found a wake-up interrupt (WINT) is generated. Setting this register to a value greater than 121 will disable the single key wake-up. The msb of this register is used to enable the serial keyboard.

The keyboard interface contains a register called the scan-code Register (ISCR). This will allow scan-codes to appear an in a PC.

Since the facility to power-down when no computer action is taking place is required, a scan counter is provided. This will count matrix scans until the count reaches the value stored in power-down Register (PDR). At this point an interrupt will occur. If the PDR is cleared then no power-down interrupt will be generated. When the PDR interrupt (PDI) is cleared, the counter will be reset. The PDR interrupt will be cleared by a read from the scan-code register or by a keyboard interrupt (KINT) occurring.

When the low Power Signal (LP) is low, all unnecessary counts will be terminated.

3-9-2 KEYBOARD CONTROLLER I/Os

SIGNAL	TYPE	DESCRIPTION
D7-0	Input	Data in
OD7-0	Output	Data out
A2-0	Input	Address
NRD	Input	Read strobe
NWR	Input	Write strobe
RST	Input	Reset
WRST	Output	Keyboard reset
KI10-0	Input	Scan input
OKI10-0	Input	Sense input
KO10-0	Output	Scan output
PDI	Output	Power down interrupt
KINT	Output	Key scan interrupts
WINT	Output	Wake-up interrupt
LP	Input	Low power mode
WAKE	Input	Not used
NTST	Input	Test mode, only used during factory test

(1) Data bus (D7-0 & OD7-0)
These are the data bus connections. D0, OD0 will correspond to bit 0 of any registers.

(2) Address inputs (A2-0)
These inputs are used to decode which registers are selected within a KRD and KWR cycle. The register decoded is as follows:

A2	A1	A0	Register	TYPE
0	0	0	SCR	R
0	0	0	ISCR	W
0	0	1	ARR	R/W
0	1	0	PDR lsb	R/W
0	1	1	PDR msb	R/W
1	0	0	WSR0	R/W
1	0	1	WSR1	R/W
1	1	0	WSR2	R/W
1	1	1	SKWR	R/W

R = Read only, W = Write only, R/W = Read/Write.
A0 is the least significant address bit.

(3) Register control lines (NRD & NWR)
When NRD is low the contents of the register addressed by A0-A2 is placed on to the data bus. The rising edge of NWR will cause the value on the data bus to be latched in to the register decoded by A0-A2.

(4) Reset line (NRST)
When NEST is Low, all keyboard registers will be cleared.

(5) WARM START (WRST)
When all the warm start scan-codes have been found on a single scan, WRST line will pulse high for one KCLK cycle. This will cause a CPU reset and will set the KRST bit in the reset source register (RSTR).

(6) Scan lines (KI10-0, OKI10-0 & KO10-0)
KO0-KO10 are the keyboard scan outputs. KI0-KI10 are the keyboard scan inputs. OKI0-OKI10 are KO0-KO10 fed back as input to the ghost key detection circuit.
At any time, one only of KO0-KO10 will be driven high. (The others will be high impedance, but are pulled down to allow Ghost Key Detection to operate)
KI0-KI10 are pulled down. Each clock cycle of KCLK will cause the examination of each of KI0-KI10 in turn. If any of KI0-KI10 are high then that KI signal combined with the high KO signal will identify a pressed key. When each of KI0-KI10 has been examined, the high KO signal is changed and the KI scan is repeated. In this way the whole key matrix will be examined, one key at a time.

(7) Interrupt signals (PDI, KINT & WINT)
PDI will go high to indicate that the power-down count has been reached. This line is cleared by reading the scan-code register or by a keyboard interrupt (KINT) occurring.
KINT will go high to indicate that a key scan-code is waiting to be read by the processor. This line is cleared by reading the scan-code from the scan-code register.
WINT will fo high for one KCLK period to indicate that the single key wake-up scan-code has been detected.

(8) Additional signals (LP, WAKE & NTST)
LP is high normally. If LP is low the keyboard circuit enters a low power mode. The ARR and PDR will stop counting to save power.
The WAKE input is unused and will be pulled high.
NTST is a test input used for testing DKI during device test.

3-9-3 KEYBOARD POWER-DOWN REGISTER PDR

This read/write 16 bit register is compared with the contents of a 16 bit counter. This counter is cleared on a key action or on writing to the PDR, and incremented each complete scan of the key board matrix if the PDR is non-zero. When the register and the counter match, a keyboard power-down interrupt is generated.

3-9-4 KEYBOARD SCAN-CODE REGISTER SCR (Read only)

Reading this read-only register after a keyboard interrupt will return a valid 8 bit scan-code. This will be held in bits 0-6, giving a scan-code between 0 and 127 (only 0-120 are valid). Bit 7 will be cleared to 0 if the interrupt was for a key press and set to 1 for a key release. Reading this register will clear the keyboard and power-down interrupts. The key matrix is mapped onto the scan-code according to the following scheme:-

Scan-code Matrix Position

HEX	DEC	SCAN	SENSE
00h	0	KO0	KI0
01h	1	KO0	KI1
.	.	.	.
0Ah	10	KO0	KT10
0Bh	11	KO1	KI0
0Ch	12	KO1	KI1
.	.	.	.
78h	120	KO10	KI10

3-9-5 PC KEYBOARD REGISTER ISCR (Write only)

This 8-bit register is write only, however it may read vi the M8255 port A (when selected). It is to be used for storing IBM format scan-codes for use wirth IRQ1.

The state of M8255 PB7 & PB6 (port B bits 7 & 6) should be checked to make sure it safe to write this register (i. e. keyboard has not been disabled by software), and IRQ1 in case the last keycode has not yet been read.

3-9-6 WARM START TRAP REGISTERS WSR0-WSR2

These are read/writeable. Each register is used to store an 8 bit scan-code. If all three of these specially selected scan-codes are found on any single complete matrix scan a warm start reset will be generated.

3-9-7 SINGLE KEY WAKE-UP REGISTER SKWR

This read/write register is used to store a 7-bit scan-code (bits 0-6). When this scan-code is found a single key wake-up interrupt is generated. Bit 7 is low to enable the on board matrix keyboard and is high to enable the external serial keyboard.

3-9-8 AUTO-REPEAT REGISTER ARR

This 8 bit read/write register holds the number of scans reguired before auto-repeat occurs. If no key strokes have occurred for this many scans and at least one key is pressed, then a periodic interrupt will be generated. This will cause the scan-code for the pressed key to be issued to the processor every scan.

3-9-9 GHOST KEY DETECTION

Since three keys or more pressed together may cause ghost keys to occur, a simple method of preventing this is required.

When the DKI detects a ghost key, it inhibits all further interrupts via KINT and preserves the state of key board matrix. After one complete scan of the keyboard matrix without a ghost key being detected, the DKI will start to generate interrupts again and will send key codes corresponding to the differences between the previous and the new state of the key matrix.

CHAPTER 5. LCD (LM64N671)

1. MAIN LCD (LM64074F)

1-1. Structure

Structure: The 640 x 200 full dot liquid display graphic display unit consists of an LCD panel, electronic component printed circuit board, and the film carrier LSI that electrically connected.

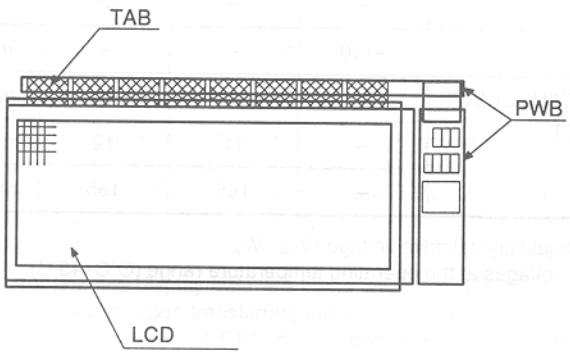


Fig. 5-1

1-2. BLOCK DIAGRAM

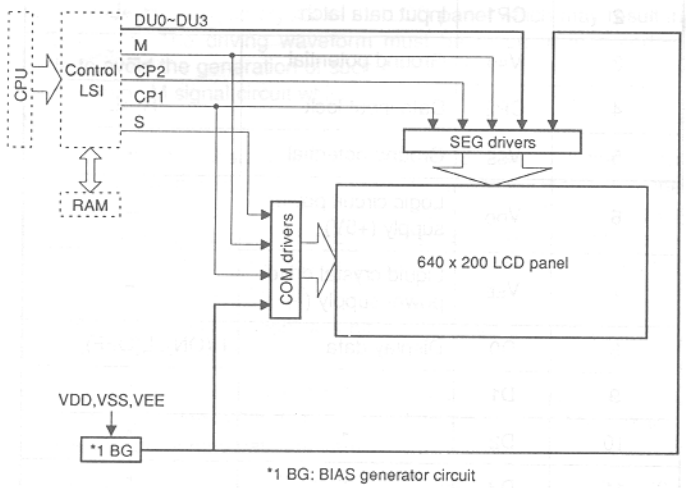


Fig. 5-2

1-3. Specification

Tbl. 5-1

Item	Characteristics	Unit
∗1 Physical dimensions	206.5(W) x 85.5(H) x 4.5MAX(D)	mm
Effective display area	177.4(W) x 70.4(H)	mm
Display format	640(W) x 200(H) full dot	–
Dot size	0.24 x 0.30	mm
Dot space	0.03	mm
∗2 Dot color	Black ∗3	–
∗2 Background color	White ∗3	–
Weight	About 68	g

∗1: The physical dimensions of the unit excludes the LCD sealed portion.
∗2: The color of the LCD panel may vary according to the environmental temperature due to the characteristic of the LCD panel.
∗3: Data "H" → ON=black
Data "L" → OFF=white

1-4. Absolute maximum rating

(1) Absolute electrical maximum rating

Tbl. 5-2

Item	Symbol	Minimum	Maximum	Unit	Note
For logic circuit	$V_{DD} - V_{SS}$	0	6.0	V	Ta = 25°C
For liquid crystal drive circuit	$V_{DD} - V_{EE}$	0	28.0	V	Ta = 25°C
Input voltage	V_{IN}	0	V_{DD}	V	Ta = 25°C

(2) Environmental requirements

Tbl. 5-3

Item	Storage		Operating		Note
	Minimum	Maximum	Minimum	Maximum	
Temperature	–25°C	+60°C	0°C	+45°C	
Humidity	NOTE(1)		NOTE(1)		Free of moisture condensation

NOTE(1): Ta ≦ 40°C . . . 95%RH, max.
Ta > 40°C . . . Absolute humidity must be 95%RH with Ta=40°C.

1-5. Electrical characteristics

(1) Electrical specification

Tbl. 5-4

Ta = 25°C, V_{DD} = 5V ± 5%

Item	Symbol	Condition	Minimum	Typical	Maximum	Note
For logic circuit supply voltage	$V_{DD} - V_{SS}$		4.75	5.0	5.25	V
For liquid crystal drive circuit supply voltage	$V_{EE} - V_{SS}$	(*1)	–6.5	–9.0	–12.3	V
Input voltage	V_{IN}	High level	0.8V_{DD}	–	V_{DD}	V
		Low level	0	–	0.2V_{DD}	V
Input leak current	I_{IL}	High level	–	–	150	µA
		Low level	–150	–	–	µA
For logic circuit supply current	I_{DD}	V_{DD}=5V, V_{DD}–V_O=F=75Hz 21.2V High frequency pattern	–	13	15	mA
For liquid crystal circuit supply current	I_{EE}		–	11	12	mA
Power consumption	Pd		–	165	185	mW

(*1): The view angle (θ) of a maximum contrast may be obtained by changing the liquid crystal drive voltage (V_{DD}–V_0).
Maximum and minimum limits of the rating show the maximum and minimum voltages at the operating temperature range (O°C~45°C).
"Typical voltage is normal voltage at 25°C.

(2) Input capacity

Tbl. 6-5

Signal name	Input capacity
S	20pF TYP
CP1	200pF TYP
CP2	200pF TYP
D0~D3	200pF TYP

(3) Interfacing signals

[1] Connector

Pin No.*	Symbol	Function	Active signal level
1	S	Scan start	"H"
2	CP1	Input data latch	H→L
3	V_{SS}	Ground potential	–
4	CP2	Data input lock	H→L
5	V_{SS}	Ground potential	–
6	V_{DD}	Logic circuit power supply (+5V)	–
7	V_{EE}	Liquid crystal drive power supply (–)	–
8	D0	Display data	H(ON), L(OFF)
9	D1	"	"
10	D2	"	"
11	D3	"	"
12	M		

Tbl. 5-6

1-6. Driving method

1) Circuit configuration

Fig.6-2 shows the block diagram of the circuit configuration.

2) Display configuration

To obtain high contrast display by decreasing the duty, the area of 640 x 200 dots display is driven by 1/200 duty.

3) Input data and control signals

The LCD driver is 80-bit LSI that consists of shift register, latch circuit and LCD drive circuit.

A 4-bit parallel data is supplied to one line (640 dots) of both display sectors at a time, starting from the upper left corner of the display, via the shift register with the clock pulse CP2.

Upon receiving one line input data (640 dots), 640 signals are latched as parallel data at a high to low transition of the latch signal CP1 to supply dot drive signals corresponding to 640 electrodes of the LCD panel.

Since the scan start signal S sent to the scan signal drive circuit has been transferred to the first line of the scan electrode, the contents of the data signals are displayed on the first line of the display screen by a combination of the LCD scan electrode and the voltage added to signal electrode.

While the first line display data are being displayed, the second line data are received. Upon transferring the 640 dots data and latched at a high to low transition of CP1, the second line data are now displayed.

When data transfer is repeated down to the 200th line in this manner using the multiplex mode from the upper to lower lines, a single cycle of a full data display (1 frame) is completed, then again starts to accept the data from the first line. The scan start signal S is a horizontal electrode drive signals.

If a DC voltage was added to the LCD panel, a chemical reaction takes place in the liquid crystal of the LCD panel which may result in LCD fatigue. The driving waveform must be reversed in a certain cycle to avoid the generation of such a DC voltage. This is performed by the async M signal circuit which converts the driving waveform into AC signal M.

On account of the characteristics of the CMOS driver LSI, the power consumption of the unit increases proportionate to the increase of the CP2 clock frequency. Therefore, to decrease the CP2 clock data transfer speed, the driver LSI incorporates the system to 4 bits transfer parallel data through 4 shift registers. Use of this LSI abates the power consumption of the unit.

For this circuit configuration, a 4-bit display data are supplied from data input lines of D0~3.

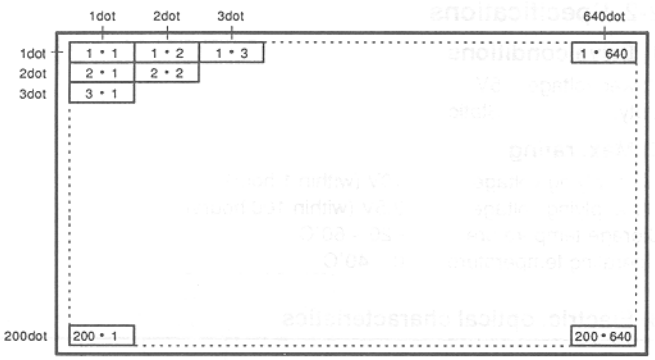
Aside from this, a data input bus line system is adopted for less power consumption. With this system, data inputs from LSI function only when appropriate data are sent.

The following shows the a full screen signal electrode data inputs and the driver LSI chip select functions.

First, when the driver LSI at the left is selected to send 80-dot data (20CP2), the right side driver close to it is selected. This action continues until the data have been sent to the driver LSI at the right. This process takes place at the same time with the signal electrode drive LSI for both screen sectors.

In this manner, data for both screen sectors are supplied through the 4-bit bus line one at a time.

Because this graphic display unit does not have the internal refresh RAM, it is necessary to supply the data and its timing pulse.



NOTE: 1·2 "1" represent the first vertical dot and "2" the second horizontal dot.

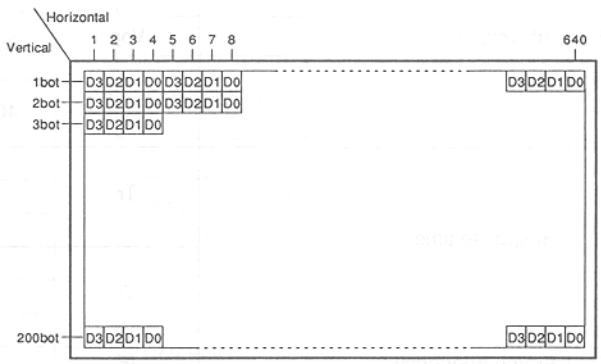


Fig. 5-5 Dot chart of Display Area

2. Static LCD

2-1. Structure

This unit is equipped with a 5-segment ON Static LCD for display of key functions.

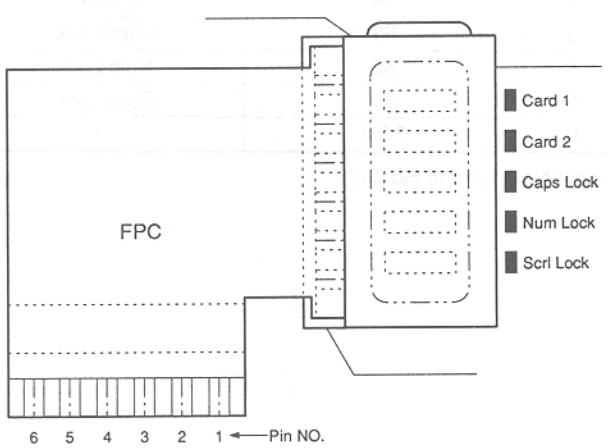


Fig. 5-6

2-2. Specifications

1) Drive conditions

Power voltage: 5V
Duty: Static

2) Max. rating

AC applying voltage: 10V (within 1 hour)
DC applying voltage: 3.5V (within 100 hours)
Storage temperature: –20 ~ 60˚C
Operating temperature: 0 ~ 40˚C

3) Electric, optical characteristics

No.	Item		Symbol	Temperature ˚C		Standard values Min.	Typ.	Max.	Unit
1	Vth voltage		Vop	0	Vth2				V
					Vth1		2.50	2.70	
				25	Vth2				
					Vth1		2.30	2.50	
				40	Vth2				
					Vth1		2.10	2.30	
2	Response time		Tr	Low temperature					ms
				0			60	90	
				25			20	30	
			Tf	Low temperature					
				0			90	140	
				25			30	50	
3	Frame frequency		fF				64		Hz
4	Capacity		C	25			1.0	1.5	nF
5	View range	Forward/Backward	θ	$\phi = 0^{\circ}$		50		80	DEG
		Right/Left	θ	$\phi = 270^{\circ}$		60		120	
6	AC current value		IAC	25			1.2	3.1	μA
7	Contrast ratio			25			5		

2-3. Interfacing signals

Pin No.	Signal name	Segment
1	S5	CARD1
2	S4	CARD2
3	S3	Caps Lock
4	S2	Num Lock
5	S1	Scrol Lock
6	COM	—

For pin Nos., refer to Fig .5-6.

CHAPTER 6. POWER SUPPLY CIRCUIT

1. Outline of the power supply

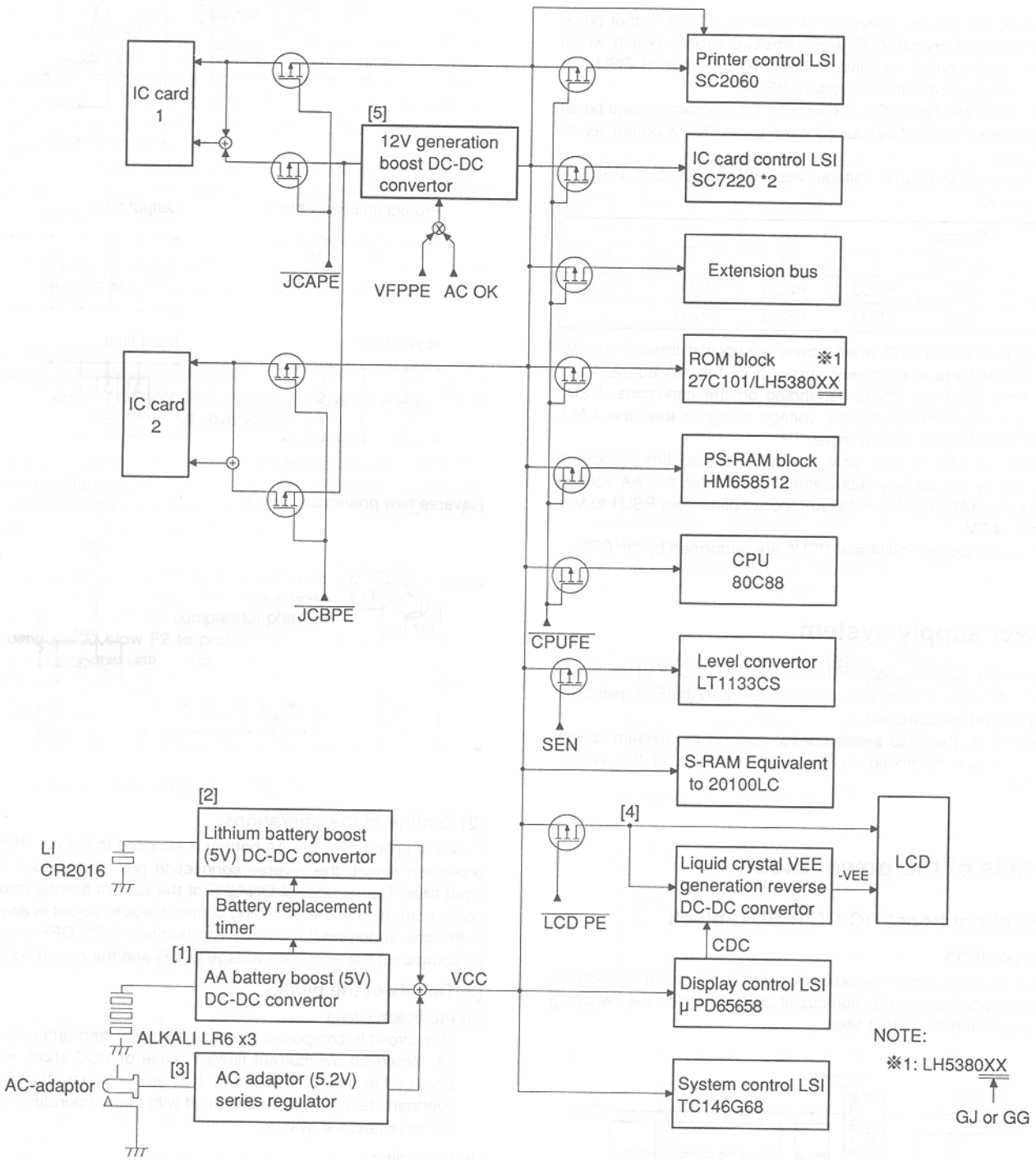


Fig. 6-1 Power supply block diagram

The power supply block is composed of five systems of input sources. The first is the pulse skip type DC-DC convertor of AA battery boost type which generates +5V inputs with three U3 batteries. (PSU1)
The second is the pulse skip type DC-DC convertor of lithium battery boost type which generates +5V input with a lithium battery CR2016. (PSU2)
The third is the series regulator (dropper) for AC adapter which generates +5.2V input with the DC power from the AC adapter. (PSU3)
The fourth is the DC-DC convertor of variable voltage output pulse skip type for liquid crystal-VEE generation/boost (back boost) which generates liquid crystal negative voltage. The output of PSU1 or PSU3 is used as input of the convertor. (PSU4)
The fifth is the PWM type DC-DC convertor for program voltage boost which generates Vpp (+12V) for IC card using PSU3 output as its input. (PSU5)
For the main power source voltage Vcc, PSU1, PSU2, or PSU3 is always inputted.

VCC source	AC input	○		×	
	AA input	○	×	○	×
LI input	YES	PSU3	PSU3	PSU1	PSU2
	NO	PSU3	PSU3	PSU1	×

Vcc is supplied from PSU3 when power is supplied through the AC adapter. When there is no power supply from the AC adapter, it is supplied from PSU1 or PSU2 depending on the conditions. PSU1 supplies Vcc when the AA battery voltage is higher than the AAFL level and Vcc is kept at 4.7V or more.
PSU2 supplies +5V to Vcc only for the specified time (about 3 minutes) set by the battery replacement timer after the AA voltage falls below the AAFL level and the voltage supplied from PSU1 to Vcc falls below +4/7V.
Operations and stop of PSU4 and PSU5 are performed by the CPU.

2. Power supply system

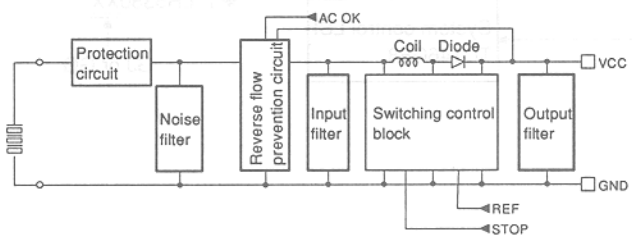
As shown in the power supply system diagram, ON/OFF of the power supplies to the operation blocks are controlled with the FET switch for reducing current consumption.
To control FETs, the CPU sends control code to the system control LSI, or FETs are controlled by the hardware logic of the system control LSI.

3. Details of the power block

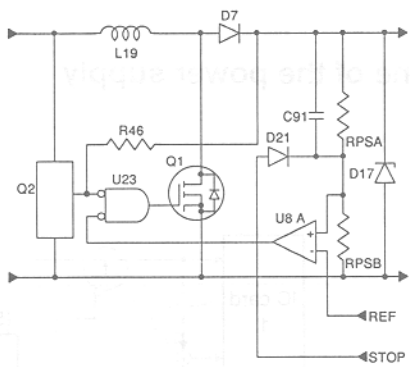
[1] AA battery boost DC-DC (PSU1) block

(1) Composition

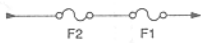
This block is composed of the protection circuit, the noise filter circuit, the reverse connection protection circuit, the input filter, the switching control circuit, and the output filter.



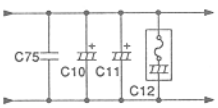
Switching control block



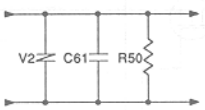
Protection circuiy block



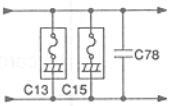
Output filter



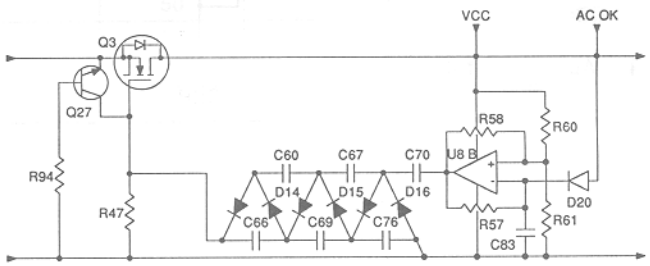
Noise filter



Input filter



Reverse flow prevention circuit



(2) Outline of the operations

Power supplied from the AA battery is supplied to the coil through the protection circuit, the reverse connection protection circuit, and the input filter. The number of ON/OFF of the current flowing through the coil is controlled in the switching control block to adjust energy stored in the coil, supplying the output. The number of ON/OFF is controlled by comparing the reference voltage (REF) and the output voltage.

(3) Details of the blocks

(a) Protection circuit

This circuit is composed of current fuse F2 and temperature fuse F1. When an overcurrent flows in case of VCC short, F2 will be blown off to protect the system. If F2 is not blown off under output overload state, F1 will be blown off with the temperature rise in the coil to protect the system.

(b) Noise filter

This block is composed of varistor V2, capacitor C61, and resistor R50. External surge is absorbed by the varistor and the capacitor to protect the internal system. R50 prevent against induction noise when a battery is not installed.

(c) Reverse connection protection circuit
This block is composed of the switch transistor FET, the oscillation comparator, the booster diode, the capacitor and the control diode.
If the battery is reversely connected, Q27 is forwardly biased to conduct Q27. The voltage between Q3 source (S) and the gate (G) becomes 0V, and Q3 is reversely biased and turned off. As a result, no voltage is supplied to the drain (D) side, protecting the system from breakage.
When the battery is properly connected, Q27 is reversely biased and turned off. At that time, power is supplied to the system by Q3's ???? diode. Then U8B starts operation to generate rectangular waveform. The output is passed to the cock craft boost circuit (D14, D15, D16, C60, C66, C69, C70, C76) to generate 10V which is applied to Q3 gate to turn on Q3. In this manner, voltage drop in Q is minimized.
When there is an AC adapter input, "H" signal is supplied through D20 to stop oscillation and reversely bias Q3, preventing a current from flowing to the battery.

(d) Input filter
This block is composed of C75, C10, C11, and C12, and absorbs noise generated in switching and reduces the impedance of the power source.

(e) Switching control block
This block is composed of oscillation IC Q2, gate IC U23, resistor R46, FET Q1, comparator U8A, voltage detection resistors PR5A and PR5B, rectifier diode D1, overvoltage preventing zenor diode D17, and control diode D21.
The divided value of the output voltage is compared with the reference voltage by the comparator U8A. When the output voltage falls below the specified value (5V), the output of Q2 in the rectangular waveform generating IC is applied to Q1 through U23 gate to switch Q1.
When Q1 is switched, energy is accumulated in L19 to overlap energy in the battery to boost the voltage level.
C91 is used to correct the comparator phase.
D17 conducts to blow F2 to protect the system when the output voltage rises abnormally.

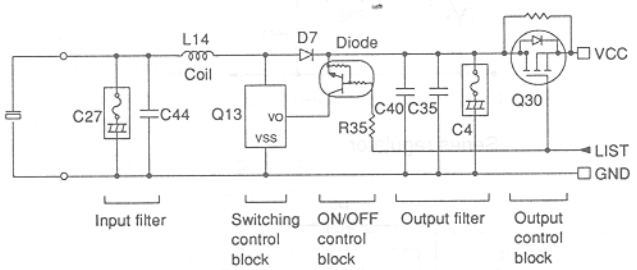
(f) Output filter
This block is composed of C75, C10, and C12.
It smoothes the waveform switched by the switching block.

[2] DC-DC for lithium battery (PSU2)

(1) Composition

As shown in Fig. 6-3, this block is composed of the input filter, the switching control block, the on/off control block, the output filter block, and the output control block.

Lithium battery boost DC-DC (PSU2)



(2) Outline of the operations

The power supplied from the lithium battery is supplied to the coil through the input filter. The number of on/off operations is controlled by the coil current switching control block to adjust the energy accumulated in the coil, adjusting the output voltage. This block operates only when the control signals (LiSTart) of the on/off control block and the output control block are active.

(3) Details of the blocks

(a) Input filter block
This block is composed of C27 and C44, absorbs noises generated by switching, and reduces impedance in the battery side.

(b) Switching block
This block is composed of the switching control IC Q13, coil L14, and diode D7. Q13 performs switching at LX pin when the voltage at VO pin falls below 5V. Energy is charged or discharged to boost, and the current is rectified in diode D7 to transmit energy to the output filter.

(c) Output filter
This block is composed of C40, C35, and C4. Energy from the switching block is accumulated and smoothed in this block.

(d) ON/OFF control block
This block is composed of digital transistor Q14 and resistor R35.
When Q14 is turned on through R35, power is supplied to the switching block to start switching. When Q14 is turned off, switching is stopped.

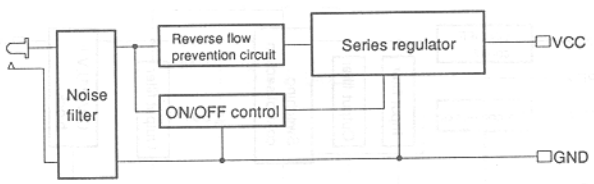
(e) Output control section
This block is composed Q30 of Pch FET.
When Q30 gate is reversely biased (+5V), Q30 is turned off and connected to VCC through the parasitic diode between the source and the drain.
When Q30 gate is forwardly biased (0V), Q13 is turned on to allow power to be supplied to VCC in small impedance.

[3] AC adapter series regulator (PSU3)

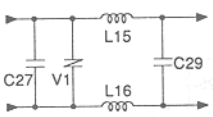
(1) Composition

This block is composed of the noise filter, the reverse flow prevention circuit, the ON/OFF control circuit, and the series regulator.

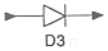
AC adaptor series regulator (PSU3)



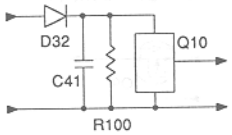
Noise filter



Reverse flow prevention circuit



ON/OFF control



(2) Outline of the operations

In this power block, an input from the DC jack is passed through the noise filter to the reverse flow prevention circuit and the ON/OFF control circuit.

In the ON/OFF circuit, the series regulator can be operative only when the input voltage is more than the specified level. the power voltage from the reverse flow prevention circuit is inputted to the series regulator, where it is stabilized and passed supplied to VCC.

(3) Details of blocks

(a) Noise filter block

This block is composed of varistor V1, capacitors C27 and C29, coils L15 and L16. External surge and noise are absorbed by the varistor, the capacitors, and the coils to protect the internal system and prevent noises in the internal system from dissipating outward.

(b) Reverse flow prevention block

This block is composed of the silicon diode D3. When a reverse voltage is applied, it is prevented by the diode to protect the system.

(c) ON/OFF control block

This block is composed of diode D32, capacitor C41, resistor R100, and voltage detection IC Q10. P32 prevent the circuit when a reverse polarity input voltage is applied. C41 prevent against malfunction and destruction caused noises. R100 protect the circuit when the input is open. Q10 (voltage detection IC) supplies HIGH level output when the input voltage rises above about 4.7V. With this signal, the series regulator block starts operation.

(e) Series regulator block

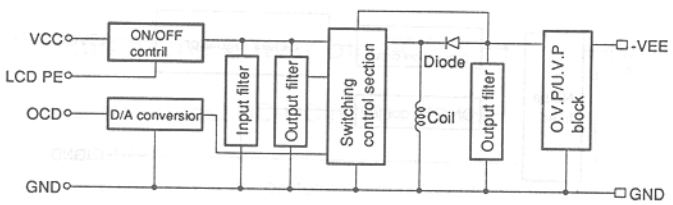
This block is composed of diode D5, D11, capacitors C45, C107, C108, transistor Q28, resistor R99, and series regulator IC U7. C107, C108, and 47 are filter capacitors to stabilize the operation of U7. D5 is a protection diode for U7. D11 is a bias setting diode. Q28 is U7 operation control transistor, which operates when Q28 is on. R99 performs to limit the Q28 base current.

[4] -VEE DC-DC (PSU4)

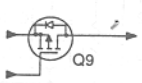
(1) Composition

This block is composed of the ON/OFF control block, the D/A convertor block, the input filter block, the reference voltage block, the switching control block, the output filter, and O.V.P/U.V.P. block

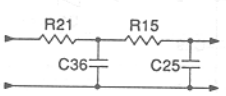
-VEE DC-DC (PSU4)



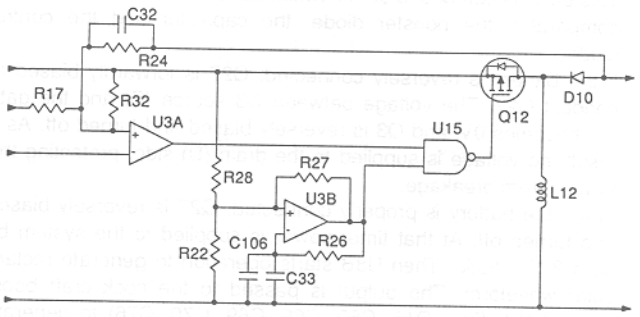
ON/OFF control



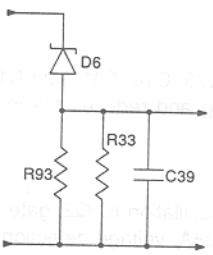
D/A conversion



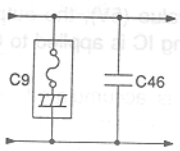
Switching control block



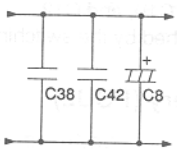
Reference voltage



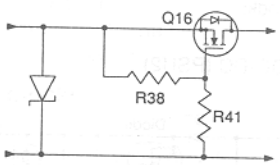
Input filter



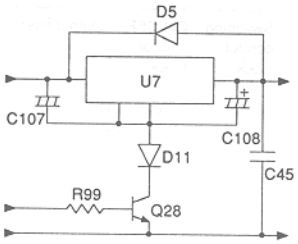
Output filter



O.V.P/U.V.P block



Series regulator



(2) Outline of operations

The ON/OFF control block controls ON/OFF of the PSU4 power. The power voltage from the control section is lowered by the power impedance in the input filter and applied to the reference voltage block and the switching control block. In the D/A conversion block, rectangular waveform duty supplied from external CDC signal is converted into a voltage. In the switching circuit block, the voltage determined with the reference voltage block output and the D/A output is compared with the output voltage (-VEE) to determine the pulse row of switching, controlling the number of switching of the coil.
Energy accumulated in the coil is varied by switching, taken out through the diode, and smoothed by the output filter to generate stabilized negative voltage. In the O.V.P/U.V.P block, the overvoltage and overcurrent protection circuit supplies -VEE only when the output filter voltage is within the specified range.

(3) details of blocks

(a) ON/OFF control block
This block is composed of PchFET Q9. When 0V is applied to Q9 gate, it is turned on and power voltage is supplied to PSU4 through the drain. In this manner, operation is started.

(b) D/A convertor block
This block is composed of resistors R21, R16, capacitors C25 and C26. In PSU$, A/D output voltage is varied by external CDC signal duty, and -VEE is also varied with that.
The given rectangular waveform (CDC) is smoothed by the integral circuit (filter) to generate a voltage according to the duty.

(e) Reference voltage block
This block is composed of zenor diode D6, resistors R93, R33, and capacitor C39.
D6 is a constant voltage diode. R39 and R33 are the bias resistors to determine the current flowing through D6. C39 functions as the filter capacitor which absorbs noises. Since D4 zenor voltage varies with temperatures, the change in temperature appears in the reference voltage, to change the output voltage (-VEE). In this manner, temperature compensation of liquid crystal density is performed.

(f) Switching control block
This block is composed of the hysteresis self-run multi-vibrator block (composed of resistors R28, R22, R27, capacitors C106, C33, and comparator IC U3B), the error amplifier block (composed of gate IC U15), switching FET Q12, rectifier diode D10, and coil L12.
U3A compares the D/A output, the reference voltage, and the out put voltage (-VEE). When -VEE is higher than the specified voltage, U3A opens gate U15 and send the rectangular waveform generated in U3B to Q12, controlling switching operation.
Q12 is the switching FET to switch the current flowing through L12. L12 stores energy with the switched current and send the energy to the output side.

(g) Input filter block
This block is composed of capacitors C9 and C46.
It absorbs switching noises and falls the impedance of the power source.

(i) O.V.P/U.V.P block
This block is composed of resistors R38, R41, NchFET Q16 and zenor diode D13.

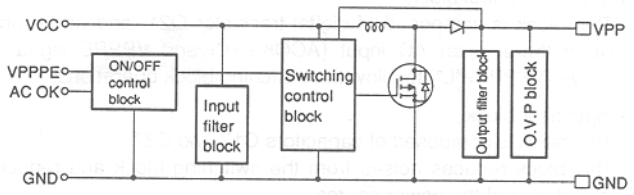
O.V.P: Over voltage protector
U.V.P: Under voltage protector

O.V.P. is composed of zenor diode D13. When the output exceeds the zenor voltage, D13 conducts to limit the generation of an overvoltage to protect the system.
U.V. P is composed of R41, R38, and Q16. The output voltage is divided by R38 and R41 to applied to Q12 gate. When this voltage is lower than the Q12 gate threshold voltage, Q16 is off to quicken the voltage drop on power off to protect the liquid crystal unit.

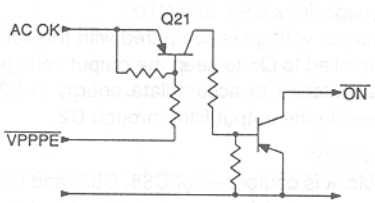
[5] VPP boost DC-DC (PSU5)

(1) Composition

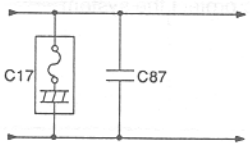
This block is composed of the ON/OFF control block, the input filter block, the switching control block, the output filter block, and the O.V.P block.



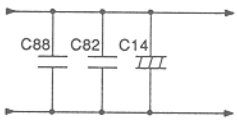
ON/OFF control block



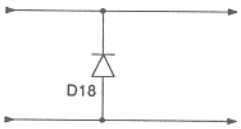
Input filter block



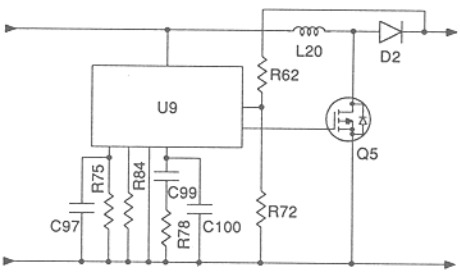
Output filter block



O.V.P block



Switching control block



(2) Outline of operations

The power voltage applied to the VCC is controlled by the switching block. Energy is stored in the coil, taken out by the diode, sent through the output filter and O.V.P to be outputted. This output (Vpp) is controlled by the ON/OFF control circuit to output +5V or +12V.

(3) Details of blocks

(a) ON/OFF control block

This block is composed of digital transistor Q21, and active only when there is an AC input (ACOK="H") and VPPPE signal is active (VPPPE="L") to allow the switching block operations.

(b) Input filter block

This block is composed of capacitors C17 and C87.

This block reduces noises from the switching block and reduces impedance of the power source.

(c) Switching block

This block is composed of oscillating frequency setting resistor R75, capacitor C97, the output voltage setting resistor R62, R72, main switching FET Q5, PWM control IC U9, U0 drive current setting resistor R84, U19 frequency characteristics setting resistor R78, capacitors C99, and C100.

The output voltage is compared with the set value to change pulse duty applied to Q5 to keep the output voltage at a constant level.

Q5 is switched to accumulate energy in L20. then the energy is supplied to the output filter through D2.

(d) Output filter

This block is composed of C88, C82, and C14.

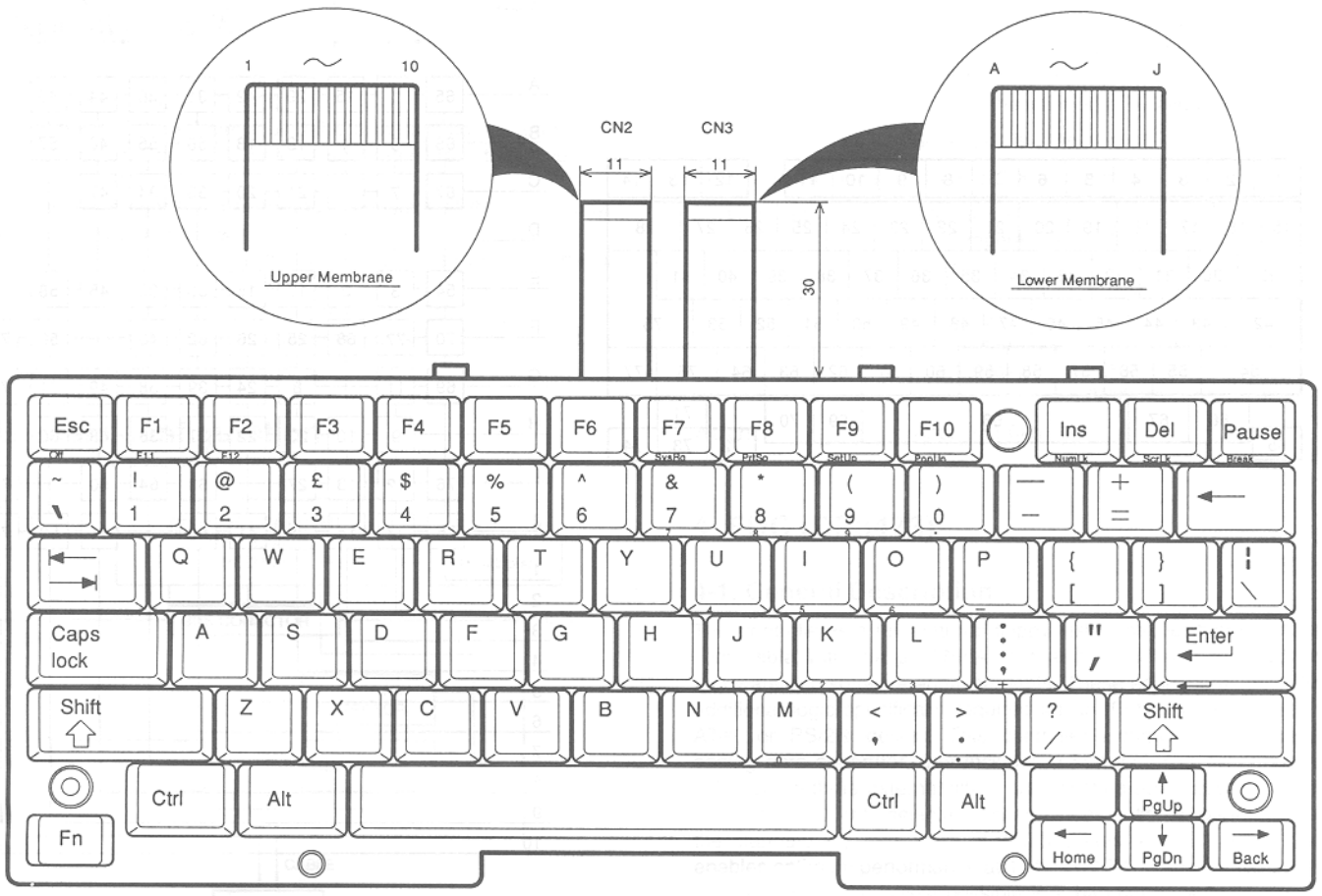
The energy sent from the switching block is stored and smoothed to provide stabilized output.

(e) O.V.P

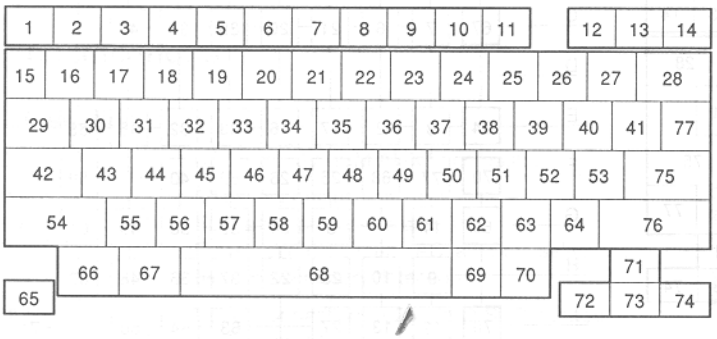
This block is composed of zenor diode D18, and absorbs an overcurrent to protect the system.

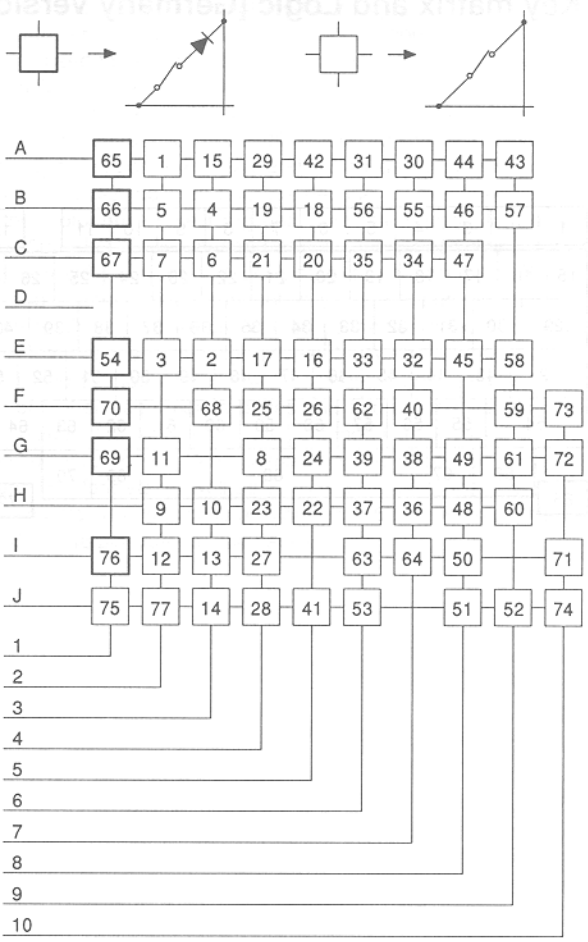
CHAPTER 7. KEYBOARD

1. External view

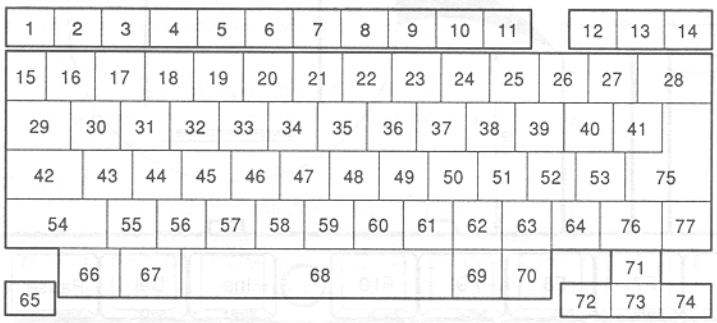


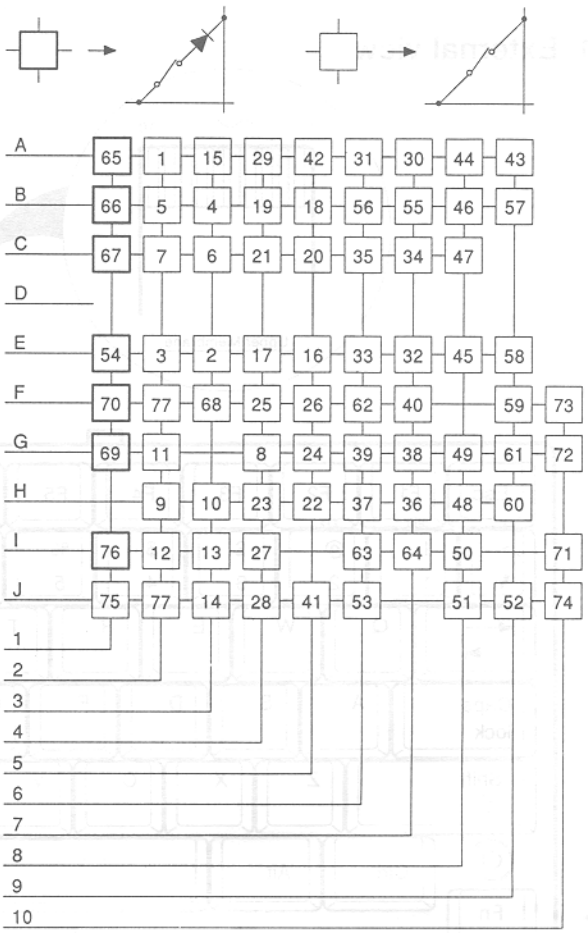
2. Key matrix and Logic [U.S Version]



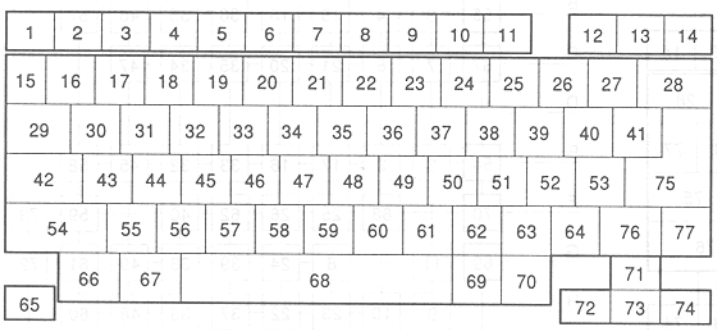


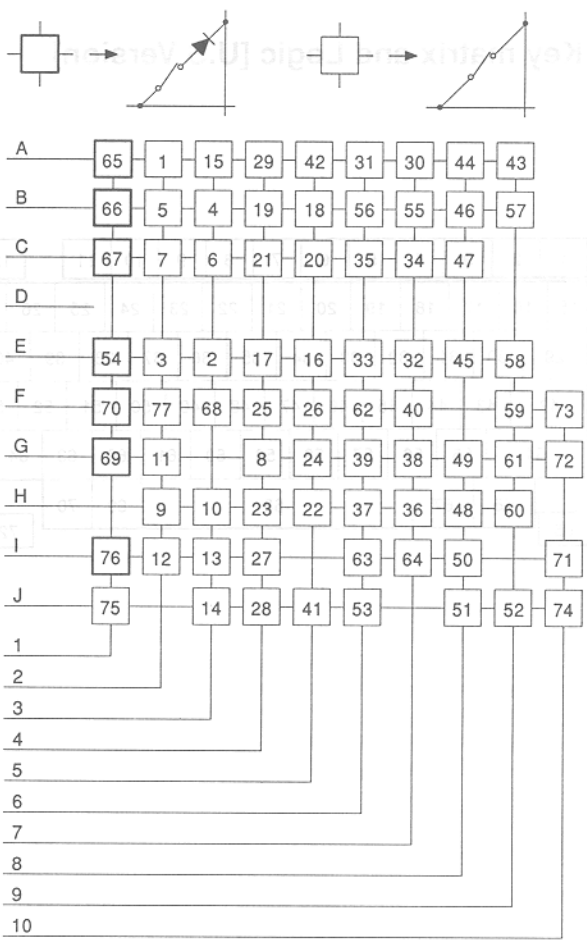
3. Key matrix and Logic [U.K Version]





2. Key matrix and Logic [Germany Version]



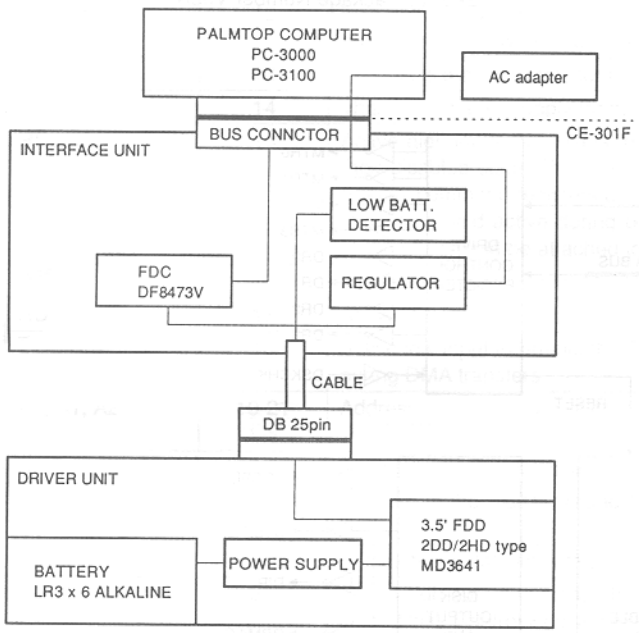


CHAPTER 8. 3.5" FDD unit (CE-301F)

1. General description

The CE-301F is an external 3.5" 2HD/2DD FDD unit for use with the palm-top computer PC-3000/3100.
It is composed of the I/F circuit and the drive unit connected with a cable each other. The cable can be separated from the drive unit side. (25 pin D-SUB)
The I/F circuit is connected to the bus connector of the main body. (Fixed manually with a screw.)
It can be driven by batteries in the drive unit. (Alkali LR3 batteries x 6).
It can be driven by AC adaptor connected to the main body.
The tilt mechanism is provided in the drive unit side. (Bezel is lifted.)

2. System configuration



3. Specifications

(1) I/F section

FDC	: NS DP8473V (IBM AT/XT compatible)
Host I/F	: 80 pin connector FDC address decode circuit Power control circuit (AC adaptor selection, battery low battery detection)
Drive connection	: Direct connection of 25 pin D-SUB connector cable (Cable length: 400mm)
External dimensions	: 98 × 60 × 20mm, excluding cable and projection

(2) Drive unit section

FDD	: CANON MD-3641 3.5" 2HD/2DD type
Power circuit	: Battery driven DC-DC circuit
Power source	: Built-in LR3 alkali batteries × 6, or AC adaptor connected to the main body. (AC adaptor input has the priority. When there is no batteries in the main body, AC adaptor is used.)
Tilt	: Bezel side is lifted about 5°.
External dimensions	: 124 × 222 × 31.5 mm
Environment	: (Operation) Temperature: 10°C ~ 35°C , Humidity: 20% ~ 30% (Without condensation) (Storage) Temperature: –20°C ~ 55°C, Humidity: 10% ~ 90% (Without condensation)
Weight	: Approx. 1.0kg

4. FDC (DP8473)

4-1. General Description

This controller is a full featured floppy disk controller that is software compatible with the µPD765A, but also includes many additional hardware and software enhancements. These enhancements include additional logic specifically required for an IBM® PC, PC-XT®, PC-AT®, or PS/2® design. This controller incorporates a precision analog data separator, that includes a self trimming delay line and VCO. Up to three external filters are switched automatically depending on the data rate selected. This provides optional performance at the standard PC data rates of 250/300 kb/s, and 500 kb/s. It also enables optimum performance at 1 Mb/s (MFM). These features combine to provide the lowest possible PLL bandwidth, with the greatest lock range, and hence the widest window margin.
This controller includes write precompensation circuitry. A shift register is used to provide a fixed 125 ns early-late precompensation for all tracks at 500k/300k/250 kb/s (83 ns for 1 MB/s), or a precompensation value that scales with the data rate, 83 ns/125 ns/208 ns/250 ns for data rates of 1.0M/500k/300k/250 kb/s respectively.
Specifically to support the PC-AT and PC-XT design, the Floppy Disk Controller PLUS-2 includes address decode for the A0-A2 address lines, the motor/drive select register, data rate register for selecting 250/300/500 kb/s, Disk Changed status, dual speed spindle motor control, low write current and DMA/interrupt sharing logic. The controller also supports direct connection to the µP bus via internal 12 mA buffers. The controller also can be connected directly to the disk drive via internal open drain high drive outputs, and Schmitt inputs.
In addition to this logic the DP8473 includes many features to ease design of higher performance drives and future controller upgrades. These include 1.0 Mb/s data rate, extended track range to 4096, Implied seeking, working Scan Commands, motor control timing, both standard IBM formats as well as Sony 3.5" (ISO) formats, and other enhancements. This device is available in a 52 pin Plastic Chip Carrier, and in a 48 pin Dual-In-Line package.

4-2. Features

- Fully μPD756A and IBM-BIOS compatible
- Integrates all PCXT®, PCAT®, and most PS/2® Logic
  - — On chip 24 MHz Crystal Oscillator
  - — DMA enable logic
  - — IBM compatible address decode of A0 ~ A2
  - — 12 mA μP bus interface buffers
  - — 40 mA floppy drive interface buffers
  - — Data rate and drive control registers
- Precision analog data separator
  - — Self-calibrating PLL and delay line
  - — Automatically chooses one of three filters
  - — Intelligent read algorithm
- Two pin programmable precompensation modes
- Other enhancements
  - — Up to 1 Mb/s data rate
  - — Implied seek up to 4000 tracks
  - — IBM or ISO formatting
- Low power CMOS, with power down mode

4-3. Connection Diagrams

Plastic Leaded Chip Carrier

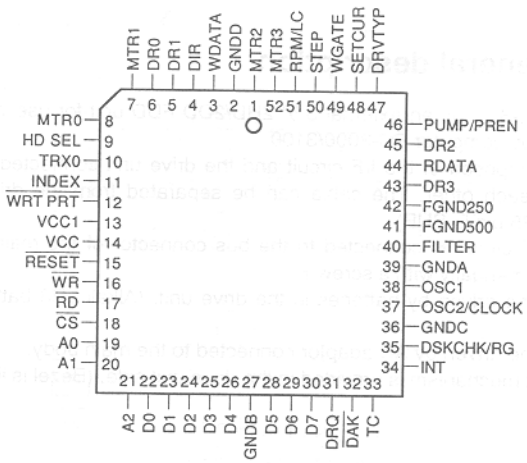
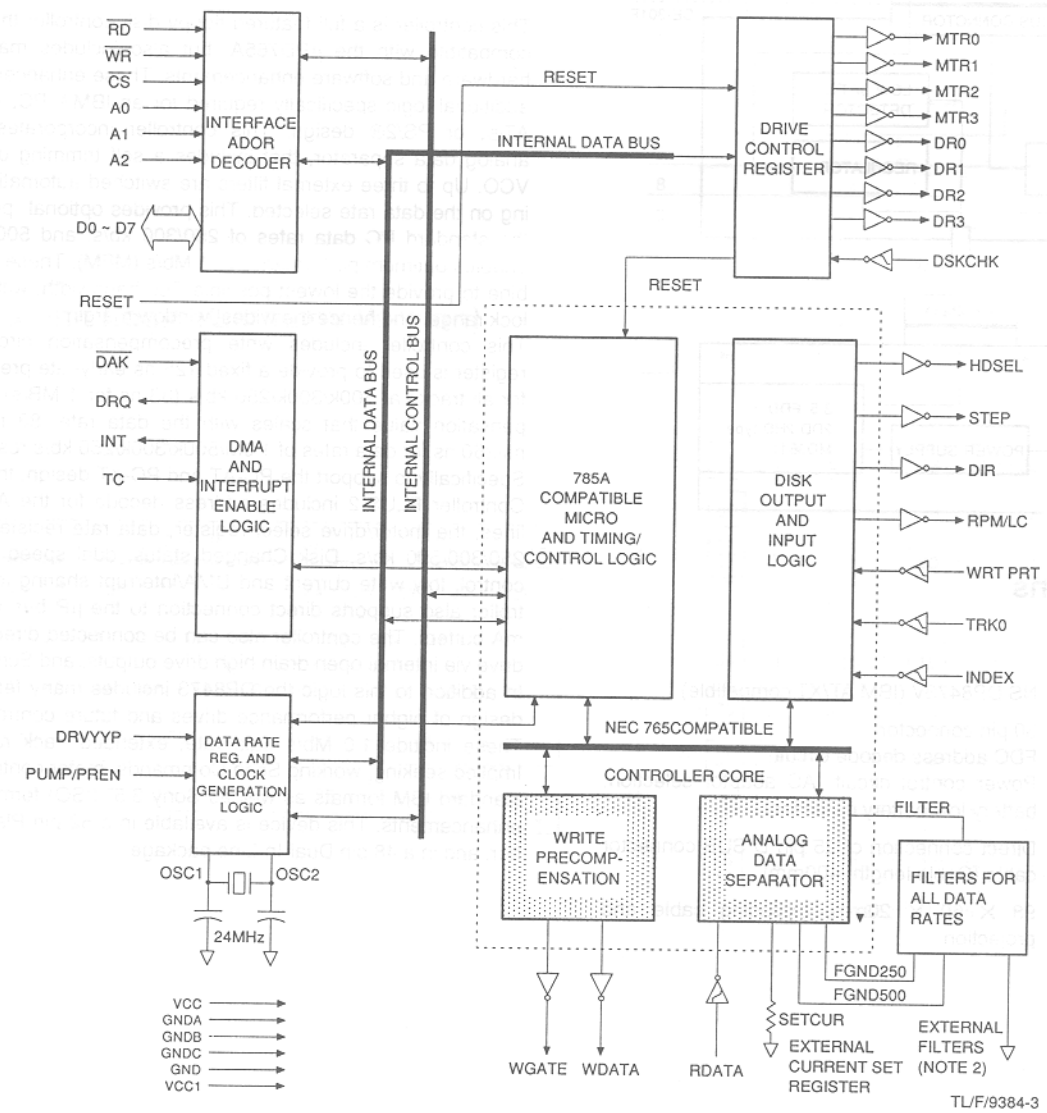


Fig. 8-2 Top View
Order Number DP8473V
See NS Package Number V52A

4-4. Block Diagram



Note 1: The MTR2, MTR3, DR2, and DR3 are not available on the 48 pin DIP (DP8473N, J) versions.
Note 2: See Figure 4 for filter description.
Note 3: Total transistor count is 29,700 (approx).

Fig. 8-3 DP8473 Functional Block Diagram

4-5. Pin Descriptions

Symbol	DP8473 PCC	Function
MTR2	1	This is an active low motor enable line for drive 2, which is controlled by the Drive Control register. This is a high drive open drain output.
GNDD	2	This pin is the digital ground for the disk interface output drivers.
WDATA	3	This is the active low open drain write precompensated serial data to be written onto the selected disk drive. This is a high drive open drain output.
DIR	4	This output determines the direction of the head movement (low = step in, high = step out). When in the write or read modes, this output will be high. This is a high drive open drain output.
DR1	5	This is an active low drive select line for drive 1 that is controlled by the Drive Control register bits D0, D1. The Drive Select bit is ANDed with the Motor Enable of the same number. This is a high drive open drain output.
DR0	6	This is an active low drive select similar to DR1 line except for drive 0.
MTR1	7	This is an active low motor enable line for drive 1. Similar to MTR2.
MTR0	8	This is an active low motor enable line for drive 0. Similar to MTR2.
HD SEL	9	This output determines which disk drive head is active. Low = Head 1, Open (high) = Head 0. This is a high drive open drain output.
TRK0	10	This active low Schmitt input tells the controller that the head is at track zero of the selected disk drive.
INDEX	11	This active low Schmitt input signal the beginning of a track.
WRT PRT	12	This active low Schmitt input indicates that the disk is write protected. Any command that writes to that disk drive is inhibited when a disk is write protected.
V_{CCA}	13	This pin is the 5V supply for the analog data separator circuitry.
V_{CC}	14	This pin in the 5V supply for the digital circuitry.
RESET	15	Active high input that resets the controller to the idle state, and resets all the output lines to the disk drive to their disabled state. The Drive Control register is reset to 00. The Data Rate register is set to 250 kb/s. The Specify command registers are not affected. The Mode Command registers are set to the default values. Reset should be held active during power up. To prevent glitches activating the reset sequence, a small capacitor (1000 pF) should be attached to this pin.
$\overline{WR}$	16	Active low input to signal a write from the microprocessor to the controller.
$\overline{RD}$	17	Active low input to signal a read from the controller to the microprocessor.
$\overline{CS}$	18	Active low input to enable the $\overline{RD}$ and $\overline{WR}$ inputs. Not required during DMA transfers. This should be held high during DMA transfers.
A0, A1, A2	19-21	Address lines from the microprocessor. This determines which registers the microprocessor is accessing as shown in Table IV in the Register Description Section. Don't care during DMA transfers.
D0-D4	22-26	Bi-directional data lines to the microprocessor. These are the lower 5 bits and have buffered 12 mA outputs.
GNDB	27	This pin is the digital ground for the 12 mA microprocessor interface buffers. This includes D-D7, INT, and DRQ.
D5-D7	28-30	Bi-directional data lines to the microprocessor. These upper 3 bits have buffered 12 mA outputs.
DRQ	31	Active high output to signal the DMA controller that a data transfer is needed. This signal is enabled when D3 of the Drive Control Register is set.
$\overline{DAK}$	32	Active low input to acknowledge the DMA request and enable the $\overline{RD}$ and $\overline{WR}$ inputs. This signal is enabled when D3 of the Drive Control Register is set.
TC	33	Active high input to indicate the termination of a DMA transfer. This signal is enabled when the DMA Acknowledge pin active.
INT	34	Active high output to signal that an operation requires the attention of the microprocessor. The action required depends on the current function of the controller. This signal is enabled when D3 of the Drive Control Register is set.
DSKCHG/RG	35	This latched Schmitt input signal is inverted and routed to D7 of the data bus and is read when address xx7H is enabled. When the RG bit in the Mode Command is set, this pin functions as a Read Gate signal that when low forces the data separator to lock to the crystal, and when high it locks to data for diagnostic purposes.
GNDC	36	This pin is the digital ground for the controller's digital logic, including all internal registers, micro-engine, etc.
OSC2/CLOCK	37	One side of the external 24 MHz crystal is attached here. If a crystal is not used, a TTL or CMOS compatible clock is connected to this pin.
OSC1	38	One side of an external 24 MHz crystal is attached here. This pin is tied low if an external clock is used.
GNDA	39	This pin is the analog ground for the data separator, including all the PLLs, and delay lines.
FILTER	40	This pin is the output of the charge pump and the input to the VCO. One or more filters are attached between this pin and the GNDA, FGND250 and FGND500 pins.
FGND500	41	This pin connects the PLL filter for 500k(MFM)/250k(FM) b/s to ground. This is a low impedance open drain output.
FGND250	42	This pin connects the PLL filter for 250k(MFM)/125k(FM) b/s or 300k(MFM)/150k(FM) b/s to ground. This is a low impedance open drain output.
DR3	43	This is the same as DR0 except for drive 3.

Symbol	DP8473 PCC	Function
RDATA	44	The active low raw data read from the disk is connected here. This is a Shmitt input.
DR2	45	This is the same as DR0 except for drive 2.
PUMP/PREN	46	When the PU bit is set in Mode Command this pin is an output that indicates when the charge pump is making a correction. Otherwise this pin is an input that sets the precomp mode as shown in Table VI. If pin is configured as PUMP, PREN is assumed high.
DRV TYP	47	This is an input used by the controller to enable the 300 kb/s mode. This enables the uses of floppy drives with either dual or single speed spindle motors. For dual speed spindle motors, this pin is tied low. When low, and 300 kb/s data rate is selected in the data rate register, the PLL actually uses 250 kb/s. This pin is tied high for single speed spindle motor drives (standard AT drive). When this pin is high and 300 kb/s is selected 300 kb/s is used. (See also RPM/LC pin).
SETCUR	48	An external resistor connected from this pin to analog ground programs the amount of charge pump current that drives the external filters. The PLL Filter Design section shows how to determine the values:
WGATE	49	This active low open drain high drive output enables the write circuitry of the selected disk drive. This output has been designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.
STEP	50	This active low open drain high drive output will produce a pulse at a software programmable rate to move the head during a seek operation.
RPM/LC	51	This high drive open drain output pin has two functions based on the selection of the DRVTYP pin. 1. When using a dual speed spindle motor floppy drive (DRVTYP pin low), this output is used to select the spindle motor speed, either 300 RPM or 360 RPM. In this mode this output goes low when 250/300 kb/data rate is chosen in the data register, an high when 500 kb/s is chosen. 2. When using a single speed spindle motor floppy drive (DRVTYP pin high), this pin indicates when to reduce the write current to the drive. This output is high for high density media (when 500 kb/s is chosen).
MTR3	52	This is an active low motor enable line for drive 3.

5. High speed switching regulator controller (TL1454C)

5-1. General description

The TL1454C is PWM system high-speed switching regulator control IC. The reference voltage circuit of 1.25V and triangular waveform oscillation circuit which allows high frequency oscillation allow perfect synchronization of two circuits. The output circuit is of totem pole output suitable for high speed operation and step-down/inverting output and step-up output are available. Its power consumption is low and operates on a low voltage, being suitable for portable unit power source.

5-2. Features

- Wide range of power voltage: 3.6V ~ 20V
- Low current consumption: 3.0mA (Typ)
- Built-in malfunction prevention circuit at low voltage
- Highly precise reference voltage source
- Timer system output short protection circuit (Built-in)
- Wide range of operating oscillation frequency allows high frequency oscillation. 50kHz ~ 2MHz
- Adjustment of stop period is possible for all duty range.

5-3. Pin arrangement (Top view)

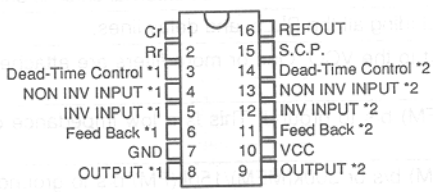
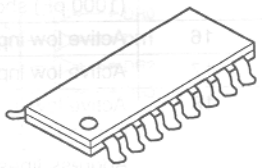


Fig. 8-4

5-4. Package external view



NS package 16 pin

Fig. 8-5

5-5. Block diagram

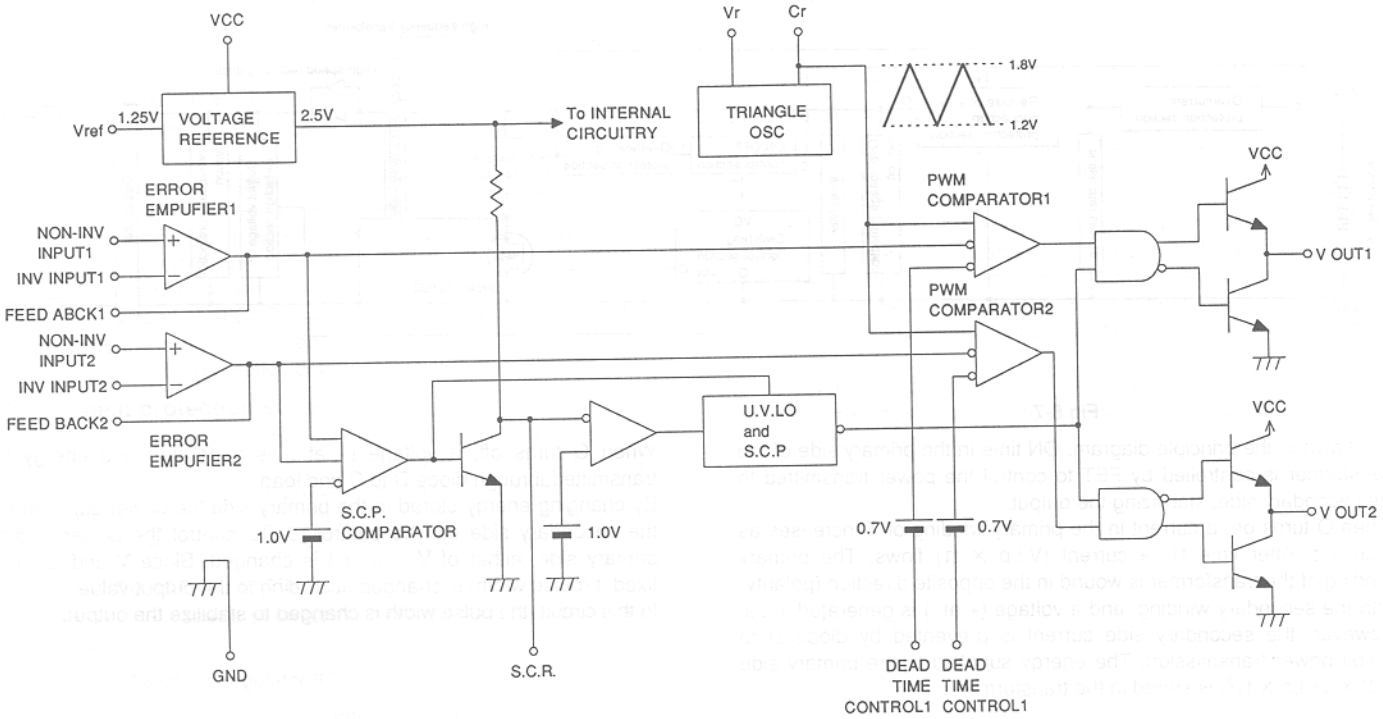


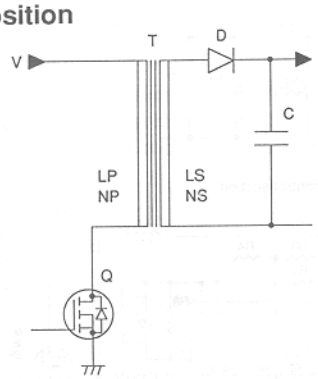
Fig. 8-6

6. DC-DC power supply

6-1. Outline of DC-DC

The DC-DC convertor section employs the PWM flyback convertor system. Six alkali manganese batteries (LR06) generate +5V output. The output can be turned on/off by external control.

6-2. Composition



The DC-DC convertor is composed of the overcurrent protection circuit, the noise filter section, the reverse polarity protection section, the overcurrent protection section, the input filter section, the ON/OFF control section, the overheating protection section, the switching control section, the snubber section, the switching FET section, the high frequency transformer, the high speed rectifying diode, the output voltage detection section, the overvoltage protection section, and the output filter section.

6-3. Operational description

Power from the batteries is passed through the overcurrent prevention section and the noise filter section where external noises are removed, and the overvoltage protection circuit to the input filter. This power is converted into intermittent current in the switching section and transmitted through the flyback transformer to the secondary side and stabilized.

To keep the output at a constant level according to the load condition, switching duty (pulse width) is varied and transmitted power is controlled.

6-4. Outline of PWM flyback DC-DC

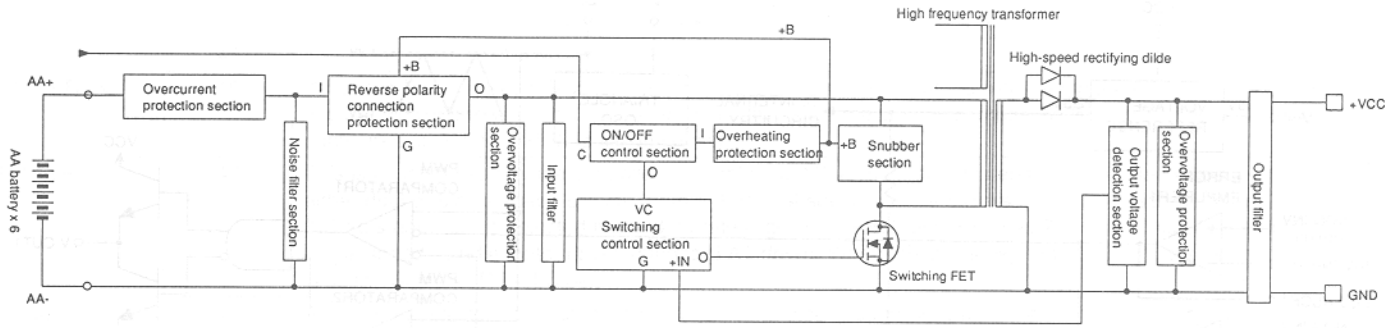


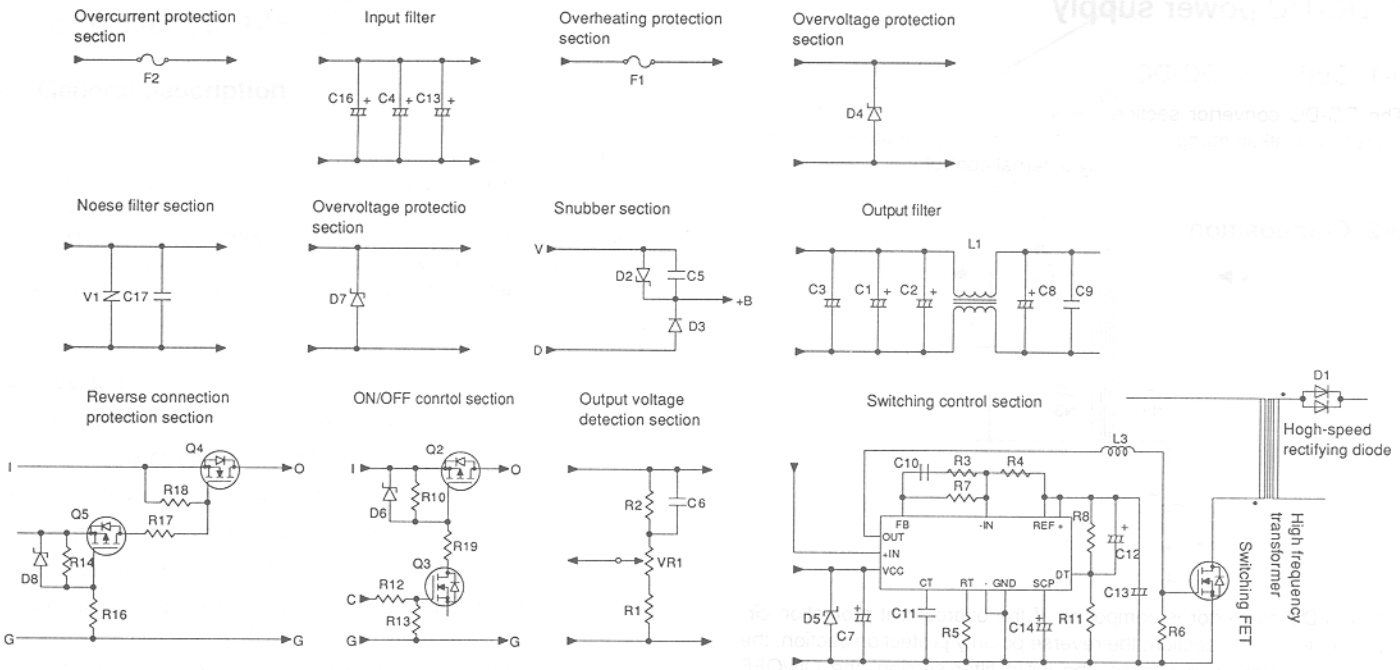
Fig 8-7

As shown in the principle diagram, ON time in the primary side of the transformer is controlled by FET to control the power transmitted to the secondary side, stabilizing the output.
When Q turns on, a current in the primary winding of T increases as V/Lp x t. After time t1, a current (V/Lp × t1) flows. The primary winding of the transformer is wound in the opposite direction (polarity) with the secondary winding, and a voltage (+ at .) is generated in Ls. However, the secondary side current is prevented by diode D to inhibit power transmission. The energy supplied to the primary side ($1/2 \times V^2/Lp \times t1^2$) is stored in the transformer.

When Q turns off, a voltage (– at .) is generated and energy is transmitted through diode D to C and load.
By changing energy stored in the primary side,the power supplied to the secondary side can be controlled. To control the power in the primary side, either of V, Lp, or t is changed. Since V and Lp are fixed, t (pulse width) is changed according to the output value.
In this circuit, the pulse width is changed to stabilize the output.

6-5. Operational description of each section

(1) Overcurrent protection circuit



This circuit is composed of the fuse. When an overcurrent flows because of breakdown of parts, the fuse is blown off to protect the system.
This part is the important part and be sure to use the specified one only.

(2) Noise filter section

This section is composed of varistor V1 and capacitor C17. The function is to absorb spike noises from external circuits and protect the system.

(3) Reverse polarity connection protection section

This section is composed of PchFET Q5, NchFET Q4, resistors R16, R18, R17, R14, and zenor diode D8. When AA battery is inserted reversely, Q5 and Q4 are reversely biased to be turned off. Therefore no reverse voltage appears in and after Q4 to protect the system. D8 is a zenor diode which prevents an overvoltage from being applied to Q5 gate. It serves as the gate protection diode. The resistors are used for bias to FET.

(4) Input filter section

This section is composed of capacitors C16, C4, and C13.
It absorbs noised in the switching section and decreases the impedance in the power line to stabilize the operations. Since a large ripple current flows through this section, capacitors of large allowable ripple current are used. (Organic semiconductor capacitors)

(5) Overvoltage protection section (Input)

This section is composed of zenor diode D7. When the input voltage exceeds the zenor voltage (12V), D7 conducts and F2 is blown off to protect the system.

(6) ON/OFF control section

This section is composed of NchFET Q3, PvhFET Q2, zenor diode D6, and resistors R12, R13, R9, and R10.
By supplying logic level signals to the control pin, ON/OFF control of the output can be performed. (C pin: Control pin)
When a voltage of 2.5V or more is applied to C pin, Q3 is turned onto pull =Q2 gate to GND and Q2 is turned on to supply power to the switching control section, which starts DC-DC operation.
When C pin is open or at GND level, Q3 and Q2 are off and no power is supplied to the switching section.
D6 zenor diode is for protection of Q2 and the resistor is for bias.

(7) Overheat protection section

This section is composed of thermal fuse F1 which is heat-connected with switching transistor Q1. When Q1 temperature rises abnormally, the fuse is blown off to cut the power supplied to the switching section and protect the system from overheat. This fuse is also an important maintenance part, and be sure to use the specified one only.

(8) Switching control section

This section is composed of switching regulator IC U1, resistors and capacitors.

U1:	Switching regulator IC
R5:	Switching frequency setting resistor
C11:	Switching frequency setting capacitor
C14:	Short protection circuit operation start time setting capacitor
R8/R11:	Dead time (Max. duty) setting resistors
C12:	Software start setting capacitor
R4/R3/R7:	Gain and frequency correction resistors
C10:	Frequency correction resistor
C13:	Reference voltage bypass capacitor
C7:	Bypass capacitor for power source
D5:	IC protection zenor diode

Outline of operation: The voltage from the output voltage detection section is compared with the reference voltage and the pulse duty applied to switching FET Q5 is changed so that the output voltage is constant.

(9) Snubber section

This section is composed of capacitor C5, diode D3, and zenor diode D2.
Since the primary side and the secondary side of the transistor are not connected 100% perfectly, a leakage inductance is generated. When energy is stored to primary side inductance Lp by switching FET ON, some energy is also stored to leakage inductance LI. When switching FET is turned off, energy stored in Lp is transmitted to Ls, but energy stored in leakage inductance is not transmitted. This will generate a high voltage in winding Np. To protect switching FET from this high voltage, the current is rectified by D3 and stored in C5 and dissipated in D2 as the form of heat. Some part of energy stored in this section is used to power the switching control section.

(10) Output voltage detection section

This section is composed of resistors R2 and R1, semi-fixed resistor VR1, and capacitor C6.
The output voltage is dropped by R2, R1, and VR1 to return to the switching section.
By adjusting VR1, the output voltage can be changed. C6 is the capacitor for phase compensation to stabilize the control system.

(11) Overvoltage protection circuit (Output side)

This section is composed of zenor diode D4. When the output voltage exceeds D4 zenor voltage, D4 conducts to operate the short-circuit prevention circuit. As a result, the output is stopped and the system is protected against an overvoltage and breakage.

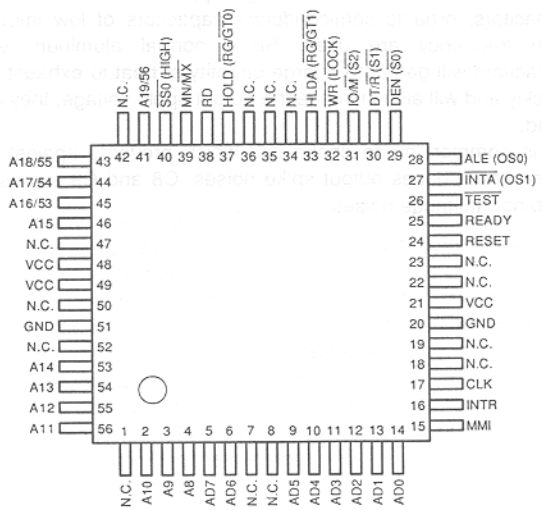
(12) Output filter section

This section is composed of electrolytic capacitors C3, C1, C2 and C8, ceramic capacitor C9, and common mode choke coil L1.
C3, C1, and C2 function to smooth the switched current to convert into an DC current. Since a large ripple current flows through the capacitors, organic semiconductor capacitors of low impedance of high frequency are used. Since normal aluminum electrolytic capacitors will generate a large quantity of heat to exhaust their lives quickly and will also increase the output ripple voltage, they cannot be used.
L1 is common mode choke coil which prevents against switching noise and reduces output spike noises. C8 and C9 are used to absorb normal mode noises.

CHAPTER 9. DESCRIPTION OF LSI'S

1. CPU (MSM80C88A-10GS)

1-1. Pin configuration



1-2. Pin description

SYMBOL	NAME	I/O	FUNCTION
AD0 ~ AD7	ADDRESS DATA BUS	Input/ Output	These lines are the multiplexed address and data bus. These are the address bus at T1 cycle and the data bus at T2, T3, TW and T4 cycle. T2, T3, TW and T4 cycle. These lines are high impedance during interrupt acknowledge and hold acknowledge.
A8 ~ A15	ADDRESS BUS	Output	These lines are the address bus bits 8 thru 15 at all cycles. These lines do not have to be latched by an ALE signal. These lines are high impedance during interrupt acknowledge and hold acknowledge.
A16/S3, A17/S4, A18/S5, A19/S6	ADDRESS/ STATUS	Output	These are the four most significant address as at the T1, cycle. Accessing I/O port address, these are low at T1 Cycles. These lines are Status lines at the T2, T3, TW and T4 Cycle. S5 indicate interrupt enable Flat. S3 and S4 are encoded as shown. S3 / S4 / Characteristics 0 / 0 / Alternate Data 1 / 0 / Stack 0 / 1 / Code or None 1 / 1 / Data These lines are high impedance during hold acknowledge.
$\overline{RD}$	READ	Output	This lines indicates that the CPU is in a memory or I/O read cycle. This line is the read strobe signal when the CPU reads data from a memory or I/O device. This line is active low. This line is high impedance during hold acknowledge.
READY	READY	Input	This line indicates to the CPU that an addressed memory or I/O device is ready to read or write. This line is active high. If the setup and hold time are out of specification, an illegal operation will occur.
INTR	INTERRUPT REQUEST	Input	This line is a level triggered interrupt request signal which is sampled during the last clock cycle of instruction and string manipulations. It can be internally masked by software. This signal is active high and internally synchronized.

<table>
<tr><th>SYMBOL</th><th>NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>$\overline{TEST}$</td><td>TEST</td><td>Input</td><td>This line is examined by a "WAIT" instruction.
When $\overline{TEST}$ is high, the CPU enters an idle cycle.
When $\overline{TEST}$ is low, the CPU exits an idle cycle.</td></tr>
<tr><td>NMI</td><td>NON MASKABLE INTERRUPT</td><td>Input</td><td>This line causes a type 2 interrupt.
NMI is not maskable.
This signal is internally synchronized and needs a 2 clock cycle pulse width.</td></tr>
<tr><td>RESET</td><td>RESET</td><td>Input</td><td>This signal causes the CPU to initialize immediately. This signal is active high and must be at least four clock cycles.</td></tr>
<tr><td>CLK</td><td>CLOCK</td><td>Input</td><td>This signal provide the basic timing for an internal circuit.</td></tr>
<tr><td>MN/$\overline{MX}$</td><td>MINIMUM/ MAXIMUM</td><td>Input</td><td>This signal selects the CPU's operate mode.
When V_{CC} is connected, the CPU operates in minimum mode.
When GND is connected, the CPU operates in maximum mode.</td></tr>
<tr><td>V_{CC}</td><td>V_{CC}</td><td></td><td>+5V supplied</td></tr>
<tr><td>GND</td><td>GROUND</td><td></td><td>The following pin function descriptions are for maximum mode only.
Other pin functions are already described.</td></tr>
<tr><td>$\overline{S0}$, $\overline{S1}$, $\overline{S2}$</td><td>STATUS</td><td>Output</td><td>These lines indicate bus status and they are used by the MSM82C88 Bus Controller to generate all memory and I/O access control signals.
These lines are high impedance during hold acknowledge.
These status lines are encoded as shown.
<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>$\overline{RQ}$/GT0
$\overline{RQ}$/GT1</td><td>REQUEST/ GRAND</td><td>Input/Output</td><td>These lines are used for Bus Request from other devices and Bus GRANT to other devices.
These lines are bidirectional and active low.</td></tr>
<tr><td>$\overline{LOCK}$</td><td>LOCK</td><td>Output</td><td>This line is active low.
When this line is low, other devices can not gain control of the bus.
This line is high impedance during hold acknowledge.</td></tr>
<tr><td>QS0/QS1</td><td>QUEUE STATUS</td><td>Output</td><td>These are Queue Status Lines that indicate internal instruction queue status.
<table>
<tr><th>QS1</th><th>QS0</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>No Operation</td></tr>
<tr><td>0</td><td>1</td><td>First Byte of Op Code from Queue</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Empty the Queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent Byte from Queue</td></tr>
</table>
The following pin function descriptions are minimum mode only. Other pin functions are already described.</td></tr>
<tr><td>IO/$\overline{M}$</td><td>STATUS</td><td>Output</td><td>This line selects memory address space or I/O address space.
When this line is low, the CPU selects memory address space and when it is high, the CPU selects I/O address space.
This line is high impedance during hold acknowledge.</td></tr>
<tr><td>$\overline{WR}$</td><td>WRITE</td><td>Output</td><td>This line indicates that the CPU is in a memory or I/O write cycle.
This line is a write strobe signal when the CPU writes data to memory or an I/O device.
This line is active low.
This line is high impedance during hold acknowledge.</td></tr>
<tr><td>$\overline{INTA}$</td><td>INTERRUPT ACKNOWLEDGE</td><td>Output</td><td>This line is a read strobe signal for the interrupt acknowledge cycle.
This line is active low.</td></tr>
<tr><td>ALE</td><td>ADDRESS LATCH ENABLE</td><td>Output</td><td>This line is used for latching an address into the MSM82C12 address latch it is a positive pulse and the trailing edge is used to strobe the address. This line in never floated.</td></tr>
<tr><td>DT/$\overline{R}$</td><td>DATA TRANSMIT/ RECEIVE</td><td>Output</td><td>This line is used to control the direction of the bus transceiver.
When this line is high, the CPU transmits data, and when it is low, the CPU receive data.
This line is high impedance during hold acknowledge.</td></tr>
<tr><td>$\overline{DEN}$</td><td>DATA ENABLE</td><td>Output</td><td>This line is used to control the output enable of the bus transceiver.
This line is active low. This line is high impedance during hold acknowledge.</td></tr>
</table>

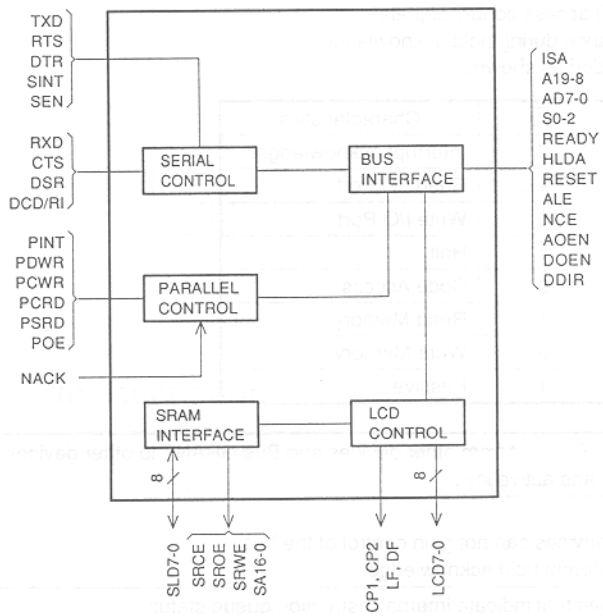
SYMBOL	NAME	I/O	FUNCTION
HOLD	HOLD REQUEST	Input	This line is used for a Bus Request from an other device. This line is active high.
HLDA	HOLD ACKNOWLEDGE	Output	This line is used for a Bus Grant to an other device.
$\overline{SS0}$	STATUS	Output	This line is logically equivalent to $\overline{S0}$ in the maximum mode.

2. DVC ASIC(μPD65658)

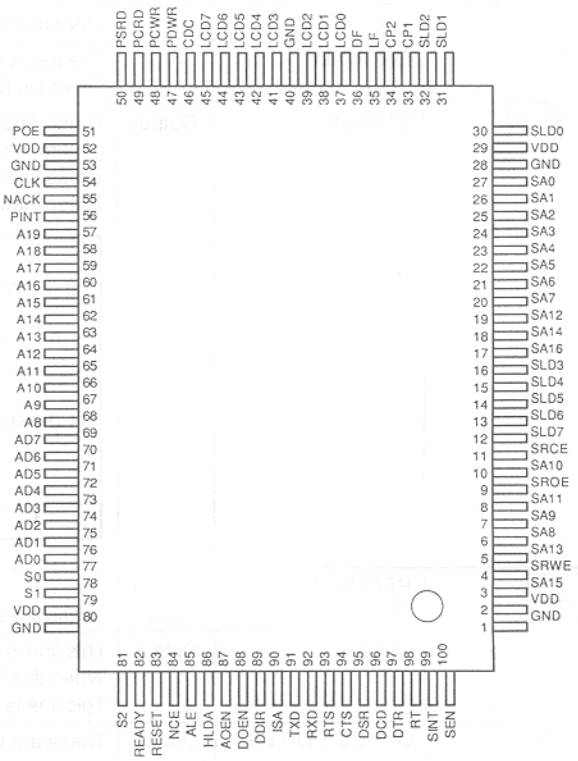
2-1. Introduction

The DVC contains a LCD controller with MDA, CGA and AT & T compatible modes, a 8250B serial controller and parallel printer port.

2-2. Block diagram



2-3. Pin configuration



2-4. Pin description

1) CPU I/F

NAME	NO.	TYPE	DESCRIPTION
ISA	1	INP	ISA bus/8088 CPU bus
A19-8	12	INP	Address
AD7-0	8	BID	Address/Data
S0-2	3	INP	CPU status/ISA IOW, IOR, MEMR Strobes
READY	1	OUT	CPU wait
HLDA	1	INP	DMA cycle in progress, (ISA AEN)
RESET	1	INP	
ALE	1	INP	
NCE	1	INP	SPC ASIC memory mapping – SA MEMW
AOEN	1	OUT	ISA Addr/Data Mux Scheme Address enable
DOEN	1	OUT	ISA Addr/Data Mux Scheme Data enable
DDIR	1	OUT	ISA Addr/Data Mux Scheme direction

(33)

2) Serial controller I/F

NAME	NO.	TYPE	DESCRIPTION
TXD	1	OUT	Transmit serial data
RXD	1	INP	Receive serial data
RTS	1	OUT	Request To Send
CTS	1	INP	Clear To Send
DSR	1	INP	Data Send Request
DCD	1	INP	Data Carrier Detect
DTR	1	OUT	Data Terminal Ready
RI	1	INP	Ring Indicator
SINT	1	OUT	Serial Controller Interrupt
SEN	1	OUT	Serial Interface Power Down

(10)

3) Parallel Printer port I/F

NAME	NO.	TYPE	DESCRIPTION
PDWR	1	OUT	Printer data write strobe
PCWR	1	OUT	Printer control write strobe
PCRD	1	OUT	Printer control read strobe
PSRD	1	OUT	Printer status read
POE	1	OUT	Printer buffer output enable
NACK	1	INP	Not printer ACK
PRINT	1	OUT	Printer port interrupt

(7)

4) SRAM I/F

NAME	NO.	TYPE	DESCRIPTION
SA16-0	17	OUT	SRAM address
SLD7-0	8	BID	SRAM data/LCD data
SRCE	1	OUT	SRAM Chip Enable
SROE	1	OUT	SRAM Output Enable
SRWE	1	OUT	SRAM Write Enable

(28)

5) LCD I/F

NAME	NO.	TYPE	DESCRIPTION
CP1	1	OUT	LCD line clock pulse
CP2	1	OUT	LCD pixel clock
LF	1	OUT	LCD line sync
DF	1	OUT	LCD frame toggle
LCD7-0	8	OUT	LCD data

(12)

6) OTHER I/F signals

NAME	NO.	TYPE	DESCRIPTION
CDC	1	OUT	Contrast voltage
CLK	1	INP	LCD Clock 10.00 Mhz

(2)

Total = (33) + (10) + (7) + (28) + (12) + (2) = 92

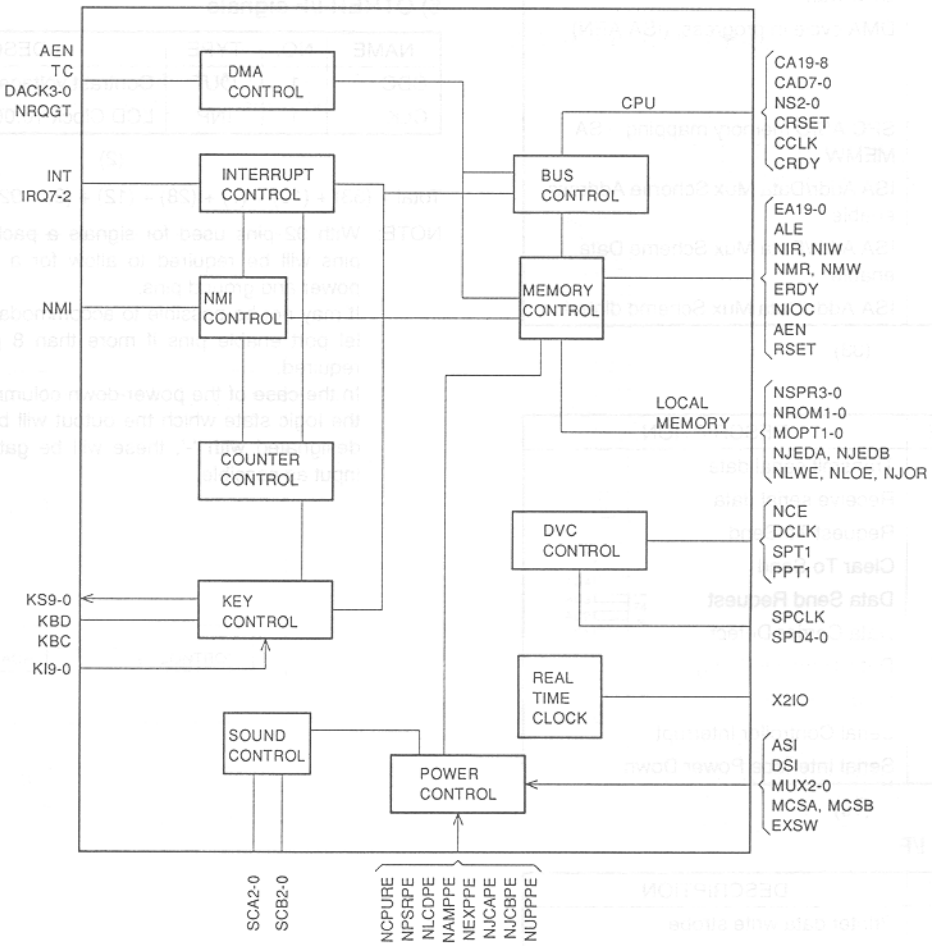
NOTE: With 92 pins used for signals a package with at least 100 pins will be required to allow for a reasonable number of power and ground pins.
It may not be possible to accommodate the serial and parallel port enable pins if more than 8 power supply pins are required.
In the case of the power-down column, the state indicated is the logic state which the output will be forced to. Inputs are designated with '-', these will be gated off as close to the input as possible.

3. SPC ASIC (TC146G68)

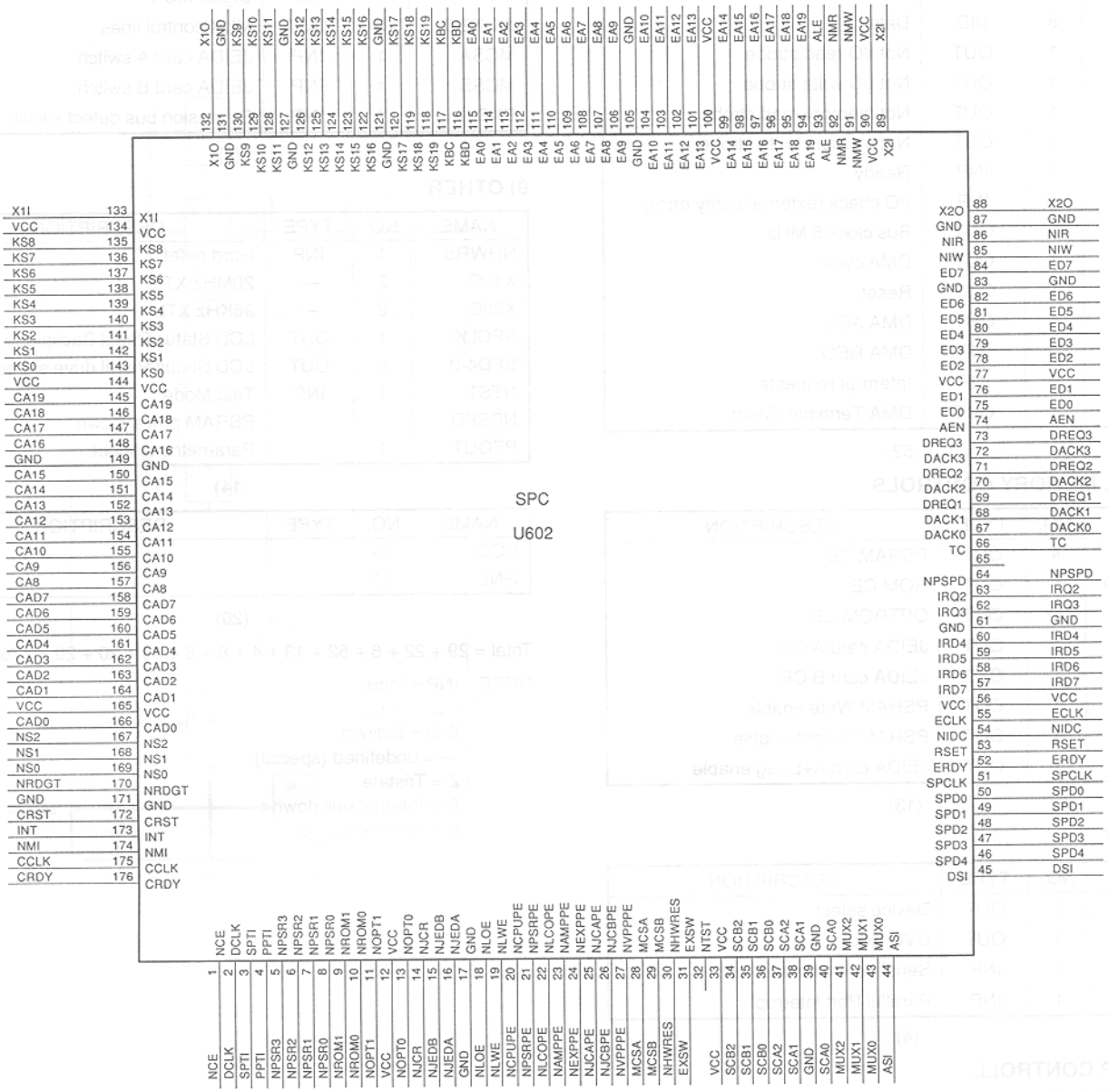
3-1. Introduction

The SPC ASIC contains all the logic needed to fully implement a PC compatible machine, in addition SPC specific logic is included.

3-2. Block diagram



3-3. Pin configuration



3-4. Pin description

1) CPU I/F

NAME	NO.	TYPE	DESCRIPTION
CA19-8	12	BID	Address
CAD7-0	8	BID	Address/Data
NS2-0	3	BID	CPU Status
NRQGT	1	BID	DMA Request/Grant
GRST	1	OUT	CPU Reset
INT	1	OUT	Interrupt
NMI	1	OUT	Non maskable interrupt
CCLK	1	OUT	Clock
CRDY	1	OUT	Ready

(29)

2) KEYBOARD

NAME	NO.	TYPE	DESCRIPTION
KS9-0	10	BID	Scan lines
KI9-0	10	INP	Sense lines
KBD	1	BID	Serial keyboard data
KBC	1	BID	Serial keyboard clock

(22)

3) SOUND

NAME	NO.	TYPE	DESCRIPTION
SCA2-0	3	OUT	Channel 1
SCB2-0	3	OUT	Channel 2

(6)

4) EXPANSION BUS

NAME	NO.	TYPE	DESCRIPTION
EA19-0	20	OUT	Address
ALE	1	OUT	Address strobe
ED7-0	8	BID	Data
NIR	1	OUT	Not I/O read strobe
NIW	1	OUT	Not I/O write strobe
NMR	1	OUT	Not memory read strobe
NMW	1	OUT	Not memory write strobe
ERDY	1	INP	Ready
NIOC	1	INP	I/O check (external parity error)
ECLK	2	OUT	Bus clock 5 MHz
AEN	1	OUT	DMA cycle
RSET	1	OUT	Reset
DACK3-0	4	OUT	DMA ACK
DREQ3-1	3	INP	DMA REQ
IRQ7-2	6	INP	Interrupt requests
TC	1	OUT	DMA Terminal Count

(52)

5) LOCAL MEMORY CONTROLS

NAME	NO.	TYPE	DESCRIPTION
NPSR3-0	4	OUT	PSRAM CE
NROM1-0	2	OUT	ROM CE
NOPT1-0	2	OUT	OPTROM CE
NJEDA	1	OUT	JEIDA card A CE
NJEDB	1	OUT	JEIDA card B CE
NLWE	1	OUT	PSRAM Write enable
NLOE	1	OUT	PSRAM Output enable
NJCR	1	OUT	JEIDA card A+B reg enable

(13)

6) DVC I/F

NAME	NO.	TYPE	DESCRIPTION
NCE	1	OUT	Device select
DCLK	1	OUT	DVC clock
SPTI	1	INP	Serial controller interrupt
PPTI	1	INP	Parallel Port interrupt

(4)

7) POWER CONTROLL

NAME	NO.	TYPE	DESCRIPTION
NCPUPE	1	OUT	CPU, ROM, Parallel Port, JEIDA Buffers
NPSRPE	1	OUT	PSRAM
NLCDPE	1	OUT	LCD
NAMPPE	1	OUT	Audio Amp
NEXPPE	1	OUT	Expansion Unit
NJCAPE	1	OUT	JEIDA card A
NJCBPE	1	OUT	JEIDA card B
NVPPPE	1	OUT	Vpp for JEIDA card B

(8)

8) SENSE LINES

NAME	NO.	TYPE	DESCRIPTION
ASI	1	INP	Level Detector
DSI	1	INP	Digital MUX
MUX2-0	3	OUT	MUX control lines
MCSA	1	INP	JEIDA card A switch
MCSB	1	INP	JEIDA card B switch
EXSW	1	INP	Expansion bus detect switch

(8)

9) OTHER

NAME	NO.	TYPE	DESCRIPTION
NHWRS	1	INP	Hard reset
X1I/O	2	—	20MHz XTL
X2I/O	2	—	96KHz XTL
SPCLK	1	OUT	LCD Status Panel Backplane
SPD4-0	5	OUT	LCD Status Panel drive signals
NTST	1	INP	Test Mode
NPSPD	1		PSRAM power down
PTOUT	1		Parametric test out

(14)

NAME	NO.	TYPE	DESCRIPTION
VCC	10		
GND	10		

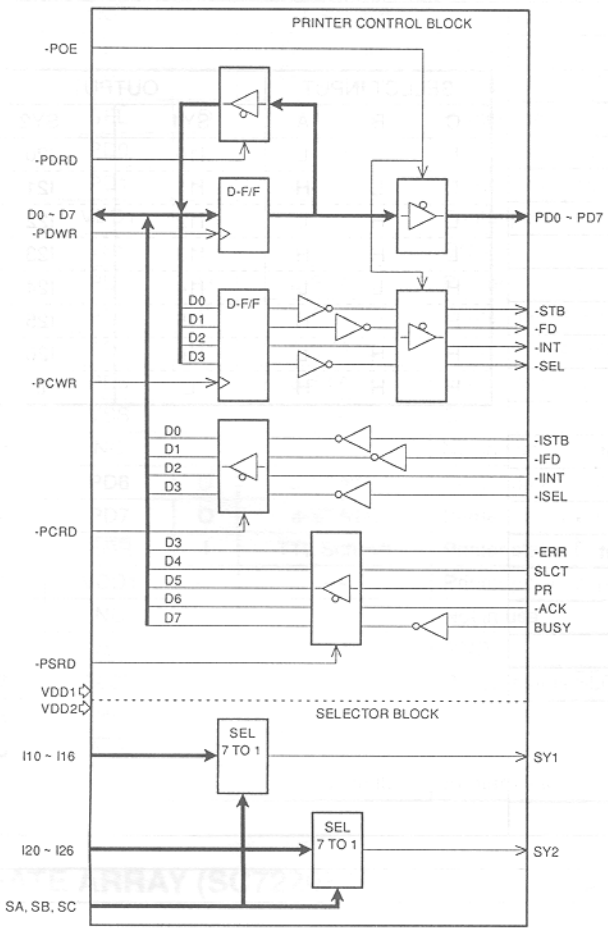
(20)

Total = 29 + 22 + 6 + 52 + 13 + 4 + 8 + 8 + 14 + 20 + 20 = 176

NOTE: INP = Input
OUT = Output
BID = Bidirect
— = undefined (special)
Z = Tristate
D = Internal pull down
U = Internal pull up

4. STANDARDCELL (SC2060FOA)

4-1. Block diagram



4-2 Pin Description

The custom CMOS IC functions as (1) printer buffer and (2) selector. Although independent power supply systems are used in function blocks (1) and (2), VDD (1) ≧ VDD (2).

● SC2060F0A terminals

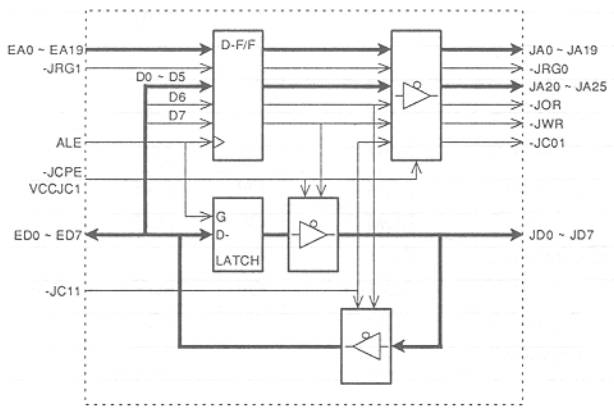
Pin No.	Signal	I/O	Buffer	Function
1	VDD2	—	—	Selector power supply
2	I10	I	CMOS Schmitt	Selector 1 input 0
3	I11	I	CMOS Schmitt	Selector 1 input 1
4	I12	I	CMOS Schmitt	Selector 1 input 2
5	VSS	—	—	GND
6	I13	I	CMOS Schmitt	Selector 1 input 3
7	I14	I	CMOS Schmitt	Selector 1 input 4
8	I15	I	CMOS Schmitt	Selector 1 input 5
9	I16	I	CMOS Schmitt	Selector 1 input 6
10	NC	—	—	Not in use
11	SA	I	CMOS Schmitt	Selector selective input A
12	SB	I	CMOS Schmitt	Selector selective input B
13	SC	I	CMOS Schmitt	Selector selective input C
14	SY1	O	Totem pole	Selector 1 selective output
15	NC	—	—	Not in use
16	VSS	—	—	GND
17	SY2	O	Totem pole	Selector 2 selective output
18	I20	I	CMOS Schmitt	Selector 2 input 0
19	I21	I	CMOS Schmitt	Selector 2 input 1
20	I22	I	CMOS Schmitt	Selector 2 input 2
21	I23	I	CMOS Schmitt	Selector 2 input 3
22	I24	I	CMOS Schmitt	Selector 2 input 4
23	I25	I	CMOS Schmitt	Selector 2 input 5
24	I26	I	CMOS Schmitt	Selector 2 input 6
25	VDD2	—	—	Selector power supply
26	VSS	—	—	GND
27	$\overline{POE}$	I	TTL	Printer output enable, active: "L"
28	PRQ	O	3-STATE	Unused
29	D0	I/O	C-MOS	CPU data 0
30	NC	—	—	Not in use
31	D1	I/O	C-MOS	CPU data 1
32	D2	I/O	C-MOS	CPU data 2
33	D3	I/O	C-MOS	CPU data 3
34	VDD1	—	—	Printer power supply
35	NC	—	—	Not in use
36	VSS	—	—	GND
37	D4	I/O	C-MOS	CPU data 4
38	D5	I/O	C-MOS	CPU data 5
39	D6	I/O	C-MOS	CPU data 6
40	D7	I/O	C-MOS	CPU data 7
41	$\overline{PDWR}$	I	TTL	Printer data write signal (data latched with)
42	$\overline{PSRD}$	I	TTL	Printer status read signal (active: "L")
43	$\overline{PCWR}$	I	TTL	Printer control write signal (data latched with)
44	$\overline{PCRD}$	I	TTL	Printer control read signal (active: "L")
45	VSS	—	—	GND
46	VDD1	—	—	Printer power supply
47	$\overline{PDRD}$	I	TTL	Unused (printer data read signal)
48	$\overline{RESET}$	I	TTL Schmitt	Printer control signal clear
49	$\overline{ISTB}$	I	TTL Schmitt	Printer control $\overline{STROBE}$ signal monitor input
50	NC	—	—	Not in use
51	$\overline{STB}$	O	Open drain	Printer control $\overline{STROBE}$ signal output
52	$\overline{IFD}$	I	TTL Schmitt	Printer control $\overline{AUTO\ FD}$ signal monitor input

SELECT INPUT			OUTPUT	
C	B	A	SY1	SY2
L	L	L	I10	I20
L	L	H	I11	I21
L	H	L	I12	I22
L	H	H	I13	I23
H	L	L	I14	I24
H	L	H	I15	I25
H	H	L	I16	I26
H	H	H	L	L

Pin No.	Signal	I/O	Buffer	Function
53	$\overline{FD}$	O	Open drain	Printer control -AUTO FD signal output
54	VDD1	—	—	Printer power supply
55	NC	—	—	Not in use
56	VSS	—	—	GND
57	$\overline{IINIT}$	I	TTL Schmitt	Printer control $\overline{INIT}$ signal monitor input
58	$\overline{INIT}$	O	Open drain	Printer control $\overline{INIT}$ signal output
59	$\overline{ISELI}$	I	TTL Schmitt	Printer control $\overline{SELECT}$ IN signal input
60	$\overline{SEL}$	O	Open drain	Printer control $\overline{SELECT\ IN}$ signal output
61	PD0	O	3-STATE	Printer data 0 output
62	PD1	O	3-STATE	Printer data 1 output
63	VDD1	—	—	Printer power supply
64	VSS	—	—	GND
65	PD2	O	3-STATE	Printer data 2 output
66	PD3	O	3-STATE	Printer data 3 output
67	PD4	O	3-STATE	Printer data 4 output
68	PD5	O	3-STATE	Printer data 5 output
69	VSS	—	—	GND
70	NC	—	—	Not in use
71	PD6	O	3-STATE	Printer data 6 output
72	PD7	O	3-STATE	Printer data 7 output
73	$\overline{ERR}$	I	TTL Schmitt	Printer status $\overline{ERROR}$ signal input
74	VDD1	—	—	Printer power supply
75	NC	—	—	Not in use
76	VSS	—	—	GND
77	SLCT	I	TTL Schmitt	Printer status $\overline{SLCT}$ input
78	PE	I	TTL Schmitt	Printer status $\overline{PE}$ input
79	$\overline{ACK}$	I	TTL Schmitt	Printer status $\overline{ACK}$ input
80	BUSY	I	TTL Schmitt	Printer status $\overline{BUSY}$ input

5. GATE ARRAY (SC7220F4E)

5-1. Block diagram



5-2. Pin Description

A custom C-MOS IC is provided for each of two IC cards as IC card interface.

Pin No.	Signal	I/O	Buffer	Function
1	VSS	—	—	GND
2	$\overline{\text{OUTE}}$	I	CMOS Schmitt	Unused, fixed at "L"
3	EA16	I	TTL	External bus address 16
4	EA17	I	TTL	External bus address 17
5	EA18	I	TTL	External bus address 18
6	EA19	I	TTL	External bus address 19
7	$\overline{\text{JRGI}}$	I	TTL	-JRG signal input from SPC
8	$\overline{\text{JCEI1}}$	I	TTL	Card select signal input from SPC
9	NC	—	—	Not in use
10	ALE	I	TTL	ALE from SPC
11	$\overline{\text{JCPE}}$	I	CMOS Schmitt	Operation enable signal for this IC; operation enabled with "L"
12	VSS	—	—	GND
13	NC	—	—	Not in use
14	JD3	I/O	Pull down	IC card data 3
15	JD4	I/O	Pull down	IC card data 4
16	JD5	I/O	Pull down	IC card data 5
17	JD6	I/O	Pull down	IC card data 6
18	JD7	I/O	Pull down	IC card data 7
19	$\overline{\text{WDE}}$	I	TTL	Data write signal from SPC to IC card
20	$\overline{\text{JCEO1}}$	O	3-STATE	IC card chip select output
21	JA10	O	3-STATE	IC card address 10
22	$\overline{\text{JOE}}$	O	3-STATE	IC card data read signal
23	JA11	O	3-STATE	IC card address 11
24	VSS	—	—	GND
25	NC	—	—	Not in use
26	VDD	—	—	Power supply
27	JA9	O	3-STATE	IC card address 9
28	JA8	O	3-STATE	IC card address 8
29	JA13	O	3-STATE	IC card address 13
30	JA14	O	3-STATE	IC card address 14
31	JA17	O	3-STATE	IC card address 17
32	JA18	O	3-STATE	IC card address 18
33	JA19	O	3-STATE	IC card address 19
34	VSS	—	—	GND
35	JA20	O	3-STATE	IC card address 20
36	JA21	O	3-STATE	IC card address 21
37	$\overline{\text{JWE}}$	O	3-STATE	IC card write signal
38	NC	—	—	Not in use
39	JA16	O	3-STATE	IC card address 16
40	JA15	O	3-STATE	IC card address 15
41	NC	—	—	Not in use
42	JA12	O	3-STATE	IC card address 12
43	VSS	—	—	GND
44	JA22	O	3-STATE	IC card address 22
45	JA23	O	3-STATE	IC card address 23
46	JA24	O	3-STATE	IC card address 24
47	JA25	O	3-STATE	IC card address 25
48	$\overline{\text{JRGO}}$	O	3-STATE	IC card attribute memory select signal
49	$\overline{\text{CLM}}$	I	CMOS Schmitt	Test terminal, fixed at "H" or "L"
50	VDD	—	—	Power supply
51	NC	—	—	Not in use
52	VSS	—	—	GND
53	JA7	O	3-STATE	IC card address 7
54	JA6	O	3-STATE	IC card address 6

Pin No.	Signal	I/O	Buffer	Function
55	JA5	O	3-STATE	IC card address 5
56	JA4	O	3-STATE	IC card address 4
57	JA3	O	3-STATE	IC card address 3
58	JA2	O	3-STATE	IC card address 2
59	JA1	O	3-STATE	IC card address 1
60	JA0	O	3-STATE	IC card address 0
61	VSS	—	—	GND
62	JD0	I/O	Pull down	IC card data 0
63	NC	—	—	Not in use
64	JD1	I/O	Pull down	IC card data 1
65	JD2	I/O	Pull down	IC card data 2
66	MM	O	Totem pole	Unused (alternating signal output)
67	NC	—	—	Not in use
68	EAO	I	TTL	External bus address 0
69	EA1	I	TTL	External bus address 1
70	EA2	I	TTL	External bus address 2
71	EA3	I	TTL	External bus address 3
72	EA4	I	TTL	External bus address 4
73	EA5	I	TTL	External bus address 5
74	EA6	I	TTL	External bus address 6
75	VSS	—	—	GND
76	VDD	—	—	Power supply
77	CP1	I	CMOS Schmitt	Unused, fixed at "L" or "H" (LCD clock)
78	SS	I	CMOS Schmitt	Unused, fixed at "L" or "H" (LCD clock)
79	VCCJC1	I	CMOS Schmitt	Power monitor terminal for IC card
80	EA7	I	TTL	External bus address 7
81	EA8	I	TTL	External bus address 8
82	EA9	I	TTL	External bus address 9
83	EA10	I	TTL	External bus address 10
84	EA11	I	TTL	External bus address 11
85	EA12	I	TTL	External bus address 12
86	EA13	I	TTL	External bus address 13
87	EA14	I	TTL	External bus address 14
88	NC	—	—	Not in use
89	EA15	I	TTL	External bus address 15
90	VSS	—	—	GND
91	NC	—	—	Not in use
92	ED0	I/O	C-MOS	External bus data 0
93	ED1	I/O	C-MOS	External bus data 1
94	ED2	I/O	C-MOS	External bus data 2
95	ED3	I/O	C-MOS	External bus data 3
96	ED4	I/O	C-MOS	External bus data 4
97	ED5	I/O	C-MOS	External bus data 5
98	ED6	I/O	C-MOS	External bus data 6
99	ED7	I/O	C-MOS	External bus data 7
100	VDD	—	—	Power supply

6. Mask ROM (LH538100)

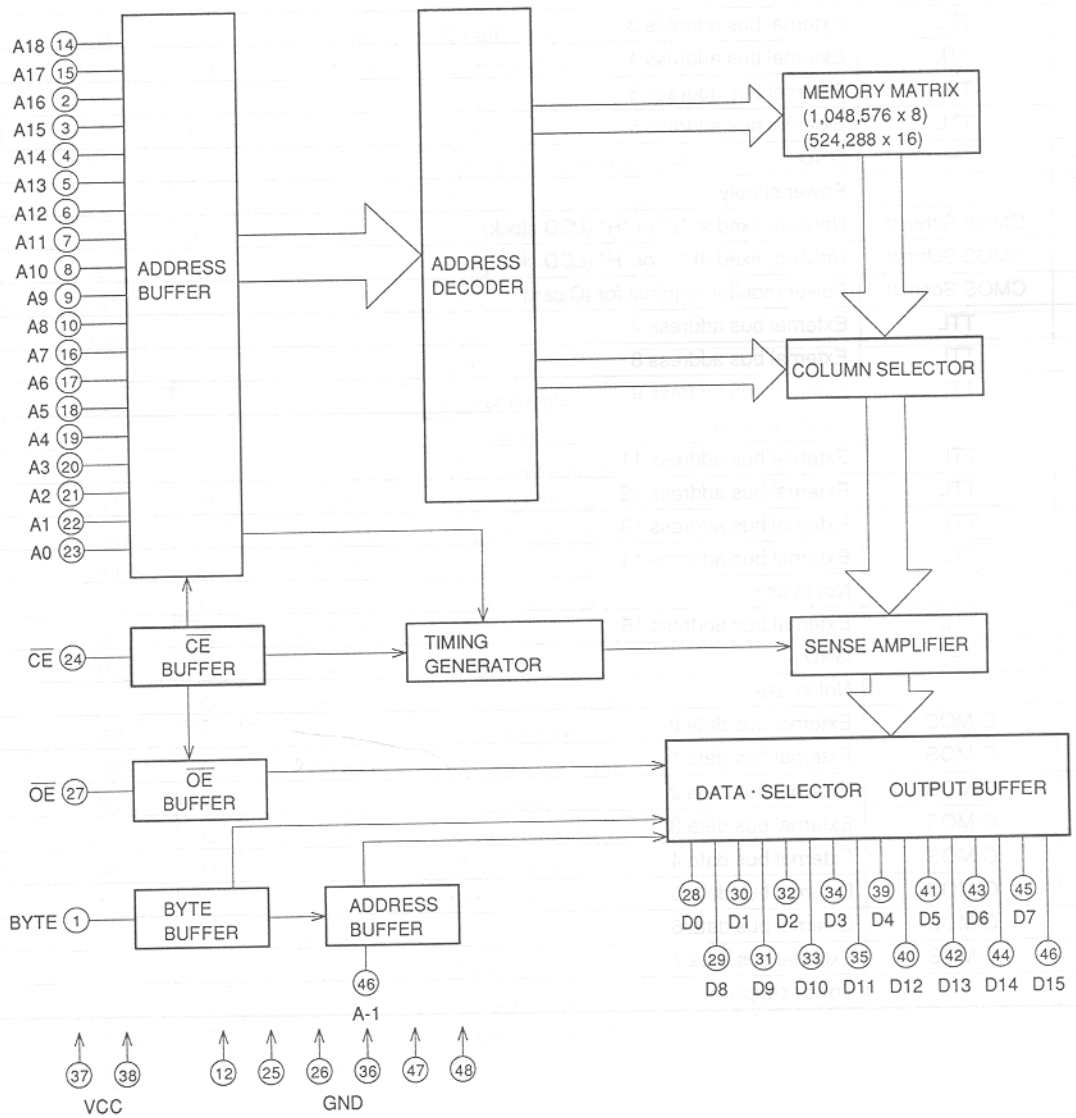
6-1. Outline

The LH538100 is an 8M-bit mask ROM manufactured by using a CMOS silicon gate process and having the following features:

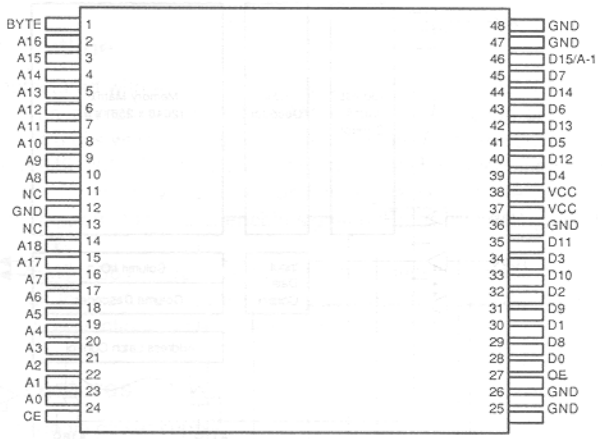
6-2. Features

- Programmable bit configuration:
  1,048,576 words × 8 bits (BYTE MODE: BYTE = V_{1L})
  524,288 words × 16 bits (WORD MODE: BYTE = V_{1H})
- Static operation (internal synchronization)
- Access time: 200 ns (max.) at Vcc = 5±10% V
- Current consumption (operation): 45 mA (max.)
- Current consumption (stand-by): 25 µA (max.) at Vcc = 5 ±20% V
- Tri-state output terminal
- Single +5 V power supply
- TTL-compatible I/O
- 48-pin, plastic TSOP

6-3. Block diagram



6-4. Pin configuration



6-5. Pin description

A-1 ~ A18	Address input
D0 ~ D15	Data output
$\overline{BYTE}$	8/16 bit (byte/word) mode-selective input
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5 V)
GND	Ground
N.C.	Non-connection (no wire bonding)

Note: Pin 46 is:
- Used as LSB (A-1) for address input when $\overline{BYTE}$ terminal (pin 1) is set to LOW level (BYTE mode).
- Used for data output (D15) when $\overline{BYTE}$ terminal (pin 1) is set to HIGH level (WORD mode).

7. OTPROM (M5M27C101VP-15)

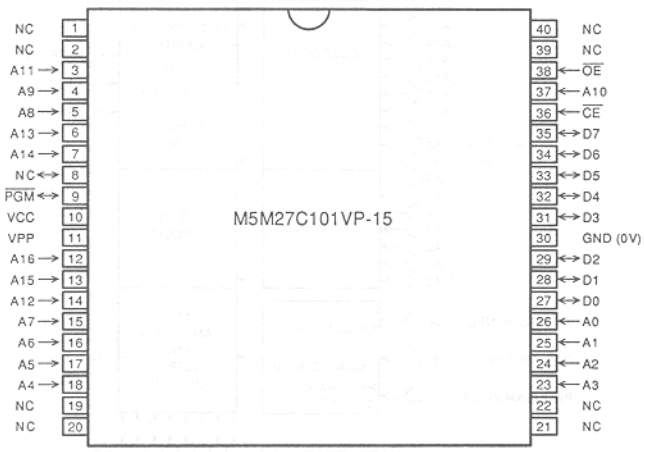
7-1. Outline

The M5M27C101VP-15 is an electrically programmable CMOS OTPROM (One-Time Programmable ROM) with a configuration of 1,048,576 bits (131,072 words × 8 bits).
The M5M27C101VP-15 is a CMOS OTPROM that is best suited for a wide range of ROM applications, including microprocessor systems. The M5M27C101VP-15 employs a EPROM (UV-erasable PROM) in a plastic package. In the EPROM, CMOS silicon gate technology is utilized for peripheral units and N channel double silicon gate technology is utilized for the memory unit.

7-2. Features

- Access time: 150 ns (max.)
- Package:
  M5M27C101VP-15: TSOP
- Static circuit
- I/O directly connectable to TTL in READ or PROGRAM mode
- Power supply:
  READ mode: 5 V single power supply
  PROGRAM mode: 12.5 V
- Programming: Byte or page programming
- JEDEC standard 32-pin DIP, PLCC
- Pin compatibility with 1M-bit EPROM (DIP, PLCC)

7-3. Pin configuration



External view

7-4. Functions

Read operation

Setting both of the $\overline{CE}$ and $\overline{OE}$ terminals to "L" and inputting address signals (using address input terminals $A_0 \sim A_{16}$) causes the stored data to be outputted from the data output terminals ($D_0 \sim D_7$). Setting either the $\overline{CE}$ or $\overline{OE}$ terminal to "H" sets the data I/O terminals to the floating status. Setting the $\overline{CE}$ terminal to "H" sets the data I/O terminals to the stand-by status (POWER DOWN mode).

Write operation

Byte programming

Setting the $\overline{CE}$ terminal to "L" and the $\overline{OE}$ terminal to "H" and applying a voltage of 12.5 V to the V_{PP} terminal activates the PROGRAM mode. The address is set with the address input terminals ($A_0 \sim A_{16}$). The data to be written is specified in 8-bit parallel with the data input terminals ($D_0 \sim D_7$). Setting the $\overline{PGM}$ terminal to "L" starts the byte programming.

Page programming

Setting the $\overline{CE}$ terminal to "H", the $\overline{OE}$ terminal to "L", and the $\overline{PGM}$ terminal to "H" and applying a voltage of 12.5 V to the V_{PP} terminal activates the PAGE DATA LATCH mode. Four different addresses are set with the address input terminals ($A_0 \sim A_{16}$). Four different data (total 4 bytes), each corresponding to the individual addresses, is specified in 8-bit parallel with the data input terminals ($D_0 \sim D_7$). At this point, the 4 bytes of data are latched in the PROM. Setting the $\overline{OE}$ terminal to "H" and the $\overline{PGM}$ terminal to "L" starts the page programming (synchronous 4-byte write operation).

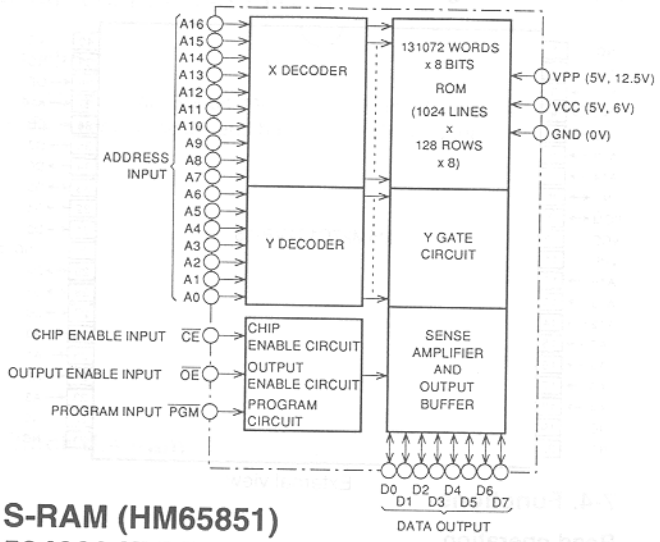
Erase operation

Data cannot be erased since the plastic package does not have a UV transmission window.

Precautions for handling

Great care should be taken to avoid an overvoltage, especially upon power-up, although a high voltage is required for write operation.

7-5. Block diagram



8. S-RAM (HM65851) 524288-Word × 8-Bit High Speed Pseudo Static RAM

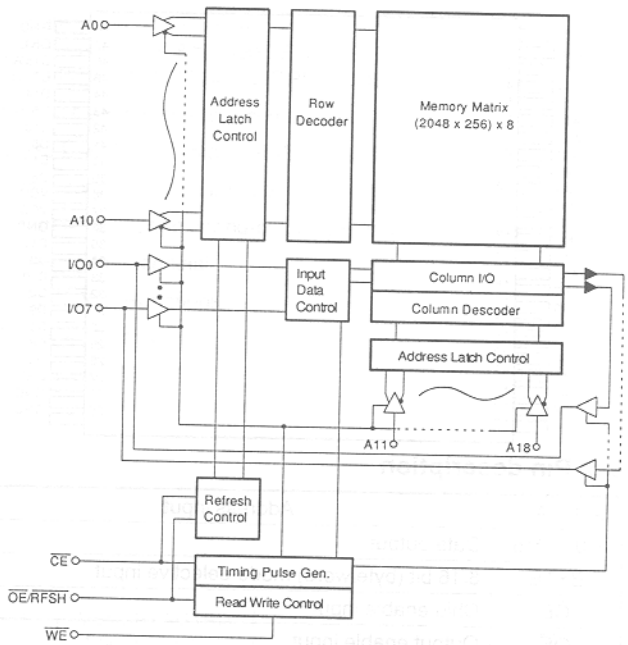
8-1. Features

- Single 5V (±10%)
- High speed
  - Access time
    $\overline{CE}$ access time: 80/100/120 ns
  - Cycle time
    Random read/write cycle time:
    160/180/210 ns
    Low power
  - 250 mW typ active
  - 350 µW typ standby (L-version)
  - 200 µW typ standby (LL-version)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
  - L-version: Address refresh
    LL-version Automatic refresh
    Self refresh
  - D-version: Address refresh
    Automatic refresh

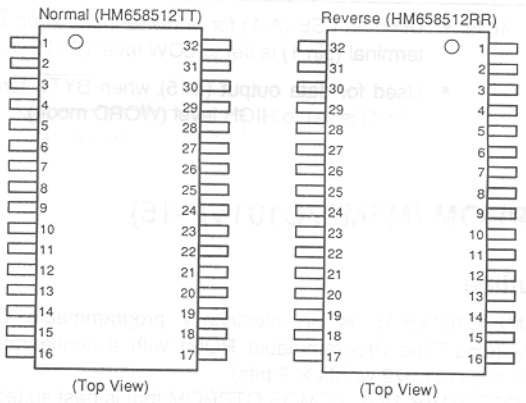
8-2. Pin Description

Pin name	Function
A0 ~ A18	Address
I/O0 ~ IO7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$/$\overline{RFSH}$	Output enable/refresh
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

8-3. Block Diagram



8-4. Pin Configuration of HM658512TT/RR



Pin No.	Pin Name
1	A18
2	A16
3	A14
4	A12
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1

Pin No.	Pin Name
12	A0
13	I/O0
14	I/O1
15	I/O2
16	VSS
17	I/O3
18	I/O4
19	I/O5
20	I/O6
21	I/O7
22	$\overline{CE}$

Pin No.	Pin Name
23	A10
24	$\overline{OE}$/$\overline{RFSH}$
25	A11
26	A9
27	A8
28	A13
29	$\overline{WE}$
30	A17
31	A15
32	VCC

Symbol	Function
A0 ~ A18	Address Inputs
I/O0 ~ I/O7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh
$\overline{WE}$	Write Enable
VCC	Power Supply
VSS	Ground

9. VRAM (M5M51008VP-12L)

9-1. Outline

Manufactured with a silicon gate CMOS process, the M5M51008VP-12L is an asynchronous static RAM with a configuration of 131,072 words × 8 bits which can operate with a single 5 V power supply.
The M5M51008VP-12L supports two types of chip select signals; the signal S_1 for memory expansion and the signal S_2 for battery back-up. It also supports the output enable signal ($\overline{OE}$) for eliminating I/O data contention.
The M5M51008VP-12L is suitable for high-density surface mounting with half the surface mounting area and less than half the thickness against conventional small out-line packages.

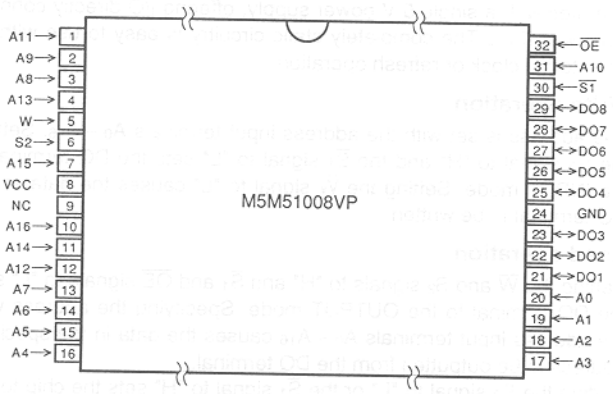
9-2. Features

- 5 V single power supply
- No external clock and refresh operation required.
- Data can be maintained with supply voltage of 2 V.
- I/O directly connectable with TTL
- Tri-state output permitting connection to OR gates
- Chip select signal for easy memory expansion
- $\overline{OE}$ input eliminating data contention on I/O bus
- Data terminal used as both an input and output terminal
- Low current consumption in stand-by status: 1.0 µA (standard value)

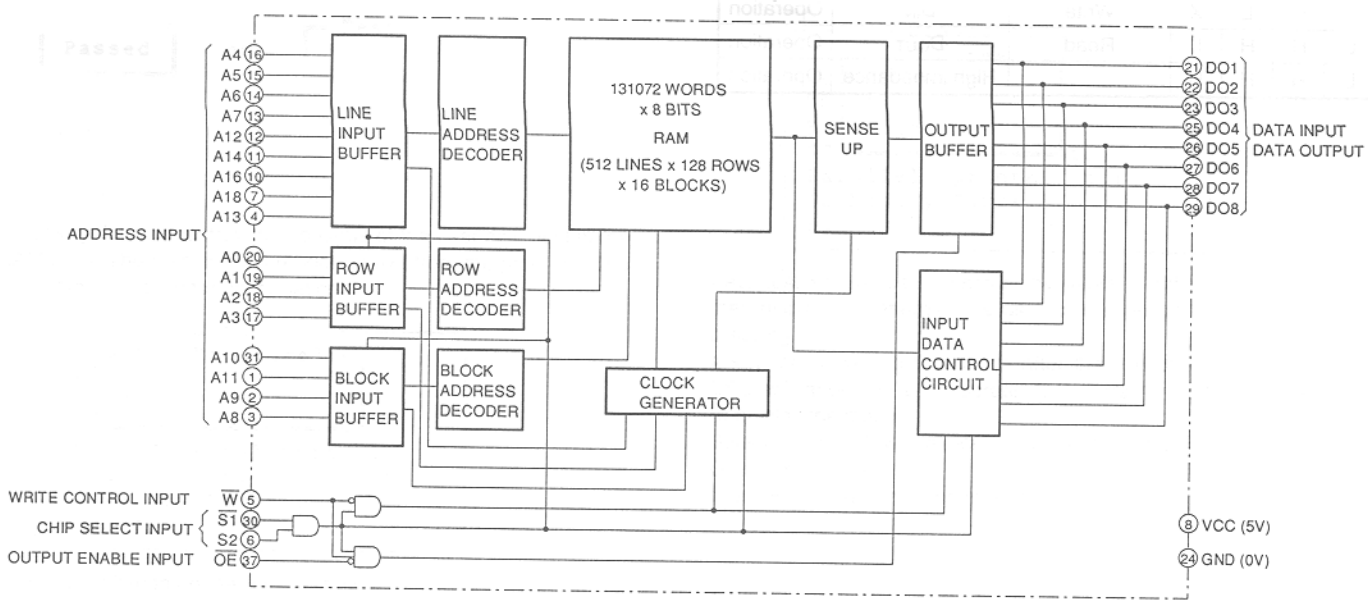
Applications

Battery drive, small storage with a battery back-up unit

9-3. Pin configuration



9-4. Block diagram



9-5. Outline

The M5M51008VP-12L with a configuration of 131,072 words × 8 bits operates with a single 5 V power supply, offering I/O directly connectable with TTL. The completely static circuitry is easy to use without an external clock or refresh operation.

Write operation

The address is set with the address input terminals $A_0 \sim A_{16}$. Setting the S_2 signal to "H" and the $\overline{S}_1$ signal to "L" sets the DQ terminal to the INPUT mode. Setting the $\overline{W}$ signal to "L" causes the data at the DQ terminal to be written.

Read operation

Setting the $\overline{W}$ and S_2 signals to "H" and $\overline{S}_1$ and $\overline{OE}$ signals to "L" sets the DQ terminal to the OUTPUT mode. Specifying the address with the address input terminals $A_0 \sim A_{16}$ causes the data in the specified address to be outputted from the DQ terminal.

Setting the S_2 signal to "L" or the $\overline{S}_1$ signal to "H" sets the chip to the non-selective status where no read/write operation can be performed. At this point, all the outputs are in the floating status (high impedance status), where connection can be established with OR gates on other chips.

Setting the $\overline{OE}$ signal to "H" sets all the outputs to the floating status. When the I/O bus method is employed, setting the $\overline{OE}$ signal to "H" during write operation can eliminate I/O data contention.

Setting the $\overline{S}_1$ signal to V_{CC} or setting the S_2 signal to GND sets all the terminals to the stand-by status. In this status, where the M5M51008VP-12L requires only a small amount of supply current (max. 1 μA), the stored data can be maintained with a supply voltage of 2 V, thus allowing battery back-up at power failure or power down in non-selective status.

Function Table

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non-selective	High impedance	Stand-by
H	X	X	X	Non-selective	High impedance	Stand-by
L	H	L	X	Write	D_{IN}	Operation
L	H	H	L	Read	D_{OUT}	Operation
L	H	H	H		High impedance	Operation

CHAPTER 10. DIAGNOSTIC

1. Outline

DIAG.EXE is a built-in program for testing hardware function. For testing, use the program according to the following procedure:

2. Command Line

DIAG /A → Automated test. Result of each test displayed.
DIAG /AQ → Automated test. Only tests which fail are displayed.
DIAG /Q → Option ignored
DIAG → Menu driven test. See section 2 onwards.

3. Menu driven tests

```
Diagnostics
CPU (Processor)
Memory
LCD screen...
Keyboard
RS-232C serial port...
Parallel (printer) port...
IC Memory Cards...
Sounds...
```

→ 3-1 Checks all processor registers.
→ 3-2 Displays size and result of memory tests.
→ 3-3 Various video tests performed.
→ 3-4 Checks each key on keyboard.
→ 3-5 Check port settings and test port.
→ 3-6 Check printer status and test port.
→ 3-7 Read/write test and Card Information.
→ 3-8 Key click, beep, tone and alarm test.

3-1. CPU (Processor)

General result displayed.

```
Test          Test
Passed   or   Failed
```

Press a key to continue.

3-2. Memory

The Memory test will destroy the contents of the user disk held in the PSRAM area. The machine will reboot on exit from the prog m. The user is therefore asked for confirmation:

```
Diagnostics
CP Are You Sure?
Me Yes
LC No
Ke
RS-232C serial port...
Parallel (printer) port...
IC Memory Cards...
Sounds...
```

The results of all memory devices is shown:

```
Diagnostics
CP Memory
Me 1024k ROM Passed
LC 128k OTPROM Failed
Ke 64k SRAM Passed
RS 1024k RAM Passed
Pa
IC Memory Cards...
Sounds...
```

Press a key to continue.

3-3. LCD Screen

Saving selected this field, another menu is displayed, as shown below.

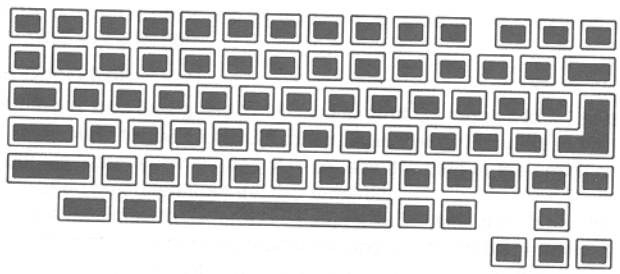
```
Diagnostics
CP LCD Screen
Me Graphics
LC Text
Ke Both
RS                t...
Parallel (printer) port...
IC Memory Cards...
Sounds...
```

Each test will exercise the screen by selecting different modes and then displaying patterns. The user can move on to the next test by pressing
a key, or by waiting 5 seconds after the end of each test. Pressing ESC will abort the LCD Screen test currently being executed and re-display the menu.
Selecting "Both" will execute all the test that are carried out in Graphics and Text.
Press ESC to return to the main menu.

3-4. Keyboard

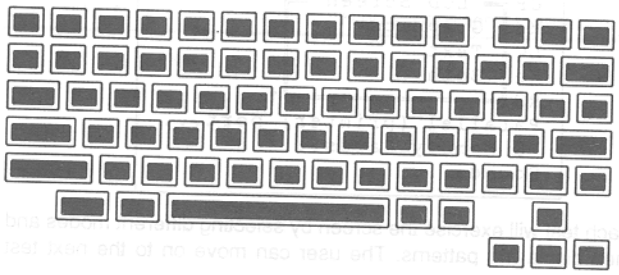
Having selected the Keyboard, the screen will display a diagram representing
the keyboard currently installed. Pressing any key will cause the corresponding key to blink while the key is held down.

For the European keyboard:



Press [ESC] twice to quit

For the USA keyboard:



Press [ESC] twice to quit

Press the ESC twice consecutively to return to main menu.
Note, this test is NOT executed during Autotest.(DIAG /A).

3-5. RS-232C serial port

A menu is displayed showing the current settings of the Serial port. The 'On line' status is re-checked only when selected by pressing RETURN.
The items below the line (Baud rate etc) are the current settings and cannot be edited.

```
Diagnostics
CP ┌ RS-232C Port ──────────┐
Me │ On line          Yes   │
LC │ Read/write test        │
Ke │ ──────────────  ─────  │
RS │ Baud Rate        110   │
Pa │ Parity          None   │
IC │ Data bits          8   │
So │ Stop bits          1   │
```

Selecting Read/Write Test is a check to see if the Serial port is working correctly. The result of the test will then be displayed as shown below.

```
Diagnostics
CP ┌ RS-232C Port ──────────┐
Me │ On ┌ Read/write test ┐Yes
LC │ Re │ Passed          │
Ke │ ── └─────────────────┘──
RS │ Baud Rate        110   │
Pa │ Parity          None   │
IC │ Data bits          8   │
So │ Stop bits          1   │
```

Please note, during Autotest, only the Read/Write Test result will be displayed.
Press ESC to return to the main menu.

3-6.Parallel port

The menu shown below is displayed.

```
Diagnostics
CP ┌ Parallel ──────┐
Me │ On line   Yes  │
LC │ Test print     │
Ke └────────────────┘
RS-232C serial port...
Parallel (printer) port...
IC Memory Cards...
Sounds...
```

Selecting "On line" wil cause the status of the attached printer to be checked.
If "Test print" is selected, an attempt will be made to print a set of characters to the attached printer. The result will be displayed as follows:-

```
Diagnostics
CP ┌ Parallel ──────┐
Me │ On ┌ Test print ┐
LC │ Te │ Passed     │
Ke └────└────────────┘
RS-232C serial port...
Parallel (printer) port...
IC Memory Cards...
Sounds...
```

3-7. IC Memory Cards

```
Diagnostics
CP ┌ Memory card ──────┐
Me │ Read/write test   │
LC │ Card information  │
Ke └───────────────────┘
RS-232C serial port...
Parallel (printer) port...
IC Memory Cards...
Sounds...
```

To carry out non-destructive test on the Memory cards installed, select "Read/Write test". The user will then be given a list of all the removable drives present to select from. Having selected the drive, the Read/Write test will be performed, and the result will be displayed.

```
Diagnostics
CP ┌ Memory card ──────┐
Me │ Re┌ Read/write test ┐
LC │ Ca│ A: drive        │
Ke └───│ B: drive        │
RS-232 └─────────────────┘
Parallel (printer) port...
IC Memory Cards...
Sounds...
```

If Card Information is selected, first a list of drives that are removable is displayed. Once the drive to check is choosen, various data relating to the card will be displayed.

```
Diagnostics
CP ┌ Sounds ┐)
Me │ Keyclick │
LC │ Beep     │
Ke │ Tone     │
RS │ Alarm    │ port...
Pa └──────────┘ter) port...
IC Memory Cards...
Sounds...
```

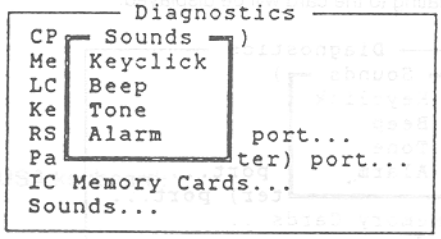
The following is an example of the data that would be displayed:

```
00      Link Target      13 03 43 49 53
05      Device type      01 03 61 fb ff
                SRAM
                Write Protect Clear
                250 nsec
0a      JEDEC ID         18 03 00 00 ff
0f      Checksum control          10 06 f1 ff 00 02 44 14
17      Version 1        15 0f 04 00 47 45 4e 45 52 49 43 00 52 41 4d 00 ff
                Version 4.0

                GENERIC
                RAM
28      Version 2        40 28 00 00 00 02 00 00 00 00 01 44 61 74 61 62 6f 6f
                         6b 2c 20 49 6e 63 2e 00 54 68 69 6e 43 61 72 64 20 64
                         72 69 76 65 73 00
                Databook, Inc.
                ThinCard drives
52      Format   41 14 00 09 00 02 00 00 00 fe 0f 00 00 02 fb 07 00 00 00 f8 0f
                 00
                 Disk
68      Geometry         42 04 00 00 00 00
6e      Data Organization         46 05 00 44 4f 53 00
75      Date     44 04 37 70 d6 16
                 14:01:46 22-06-1991
7b      Battery Replacement       45 04 00 00 00 00
                 00-00-1980
                 00-00-1980
81      End of List      ff 00
```

Only the Read/Write test will be carried out for Autotest (DIAG /A) for all the removable drives present.

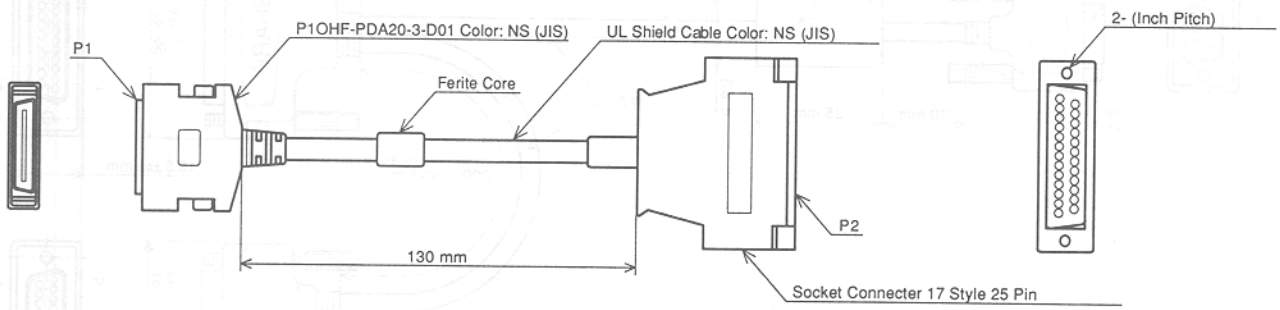
3-8. Sounds



Various forms of sound tests can be selected as shown above. Each test will last 5 seconds. During this time, the message "Working..." will be displayed.
Pressing ESC will abort the current test, and the Sound menu will be redisplayed.

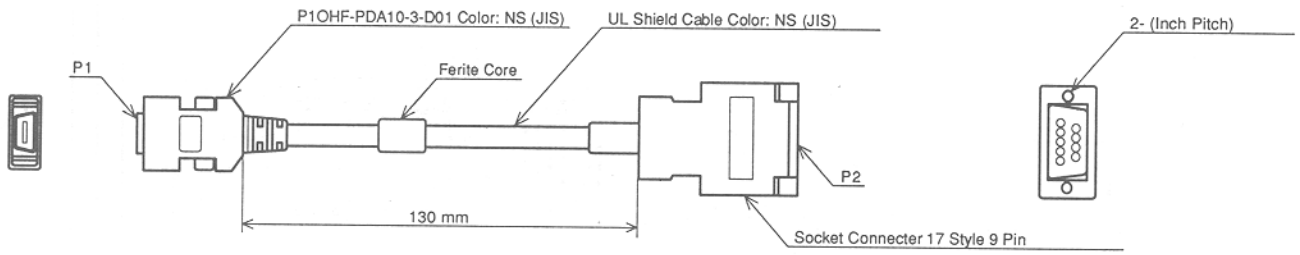
CHAPTER 11. OPTIONS

1. CE-301CB [for Printer] – Standard option of U.Y Version –



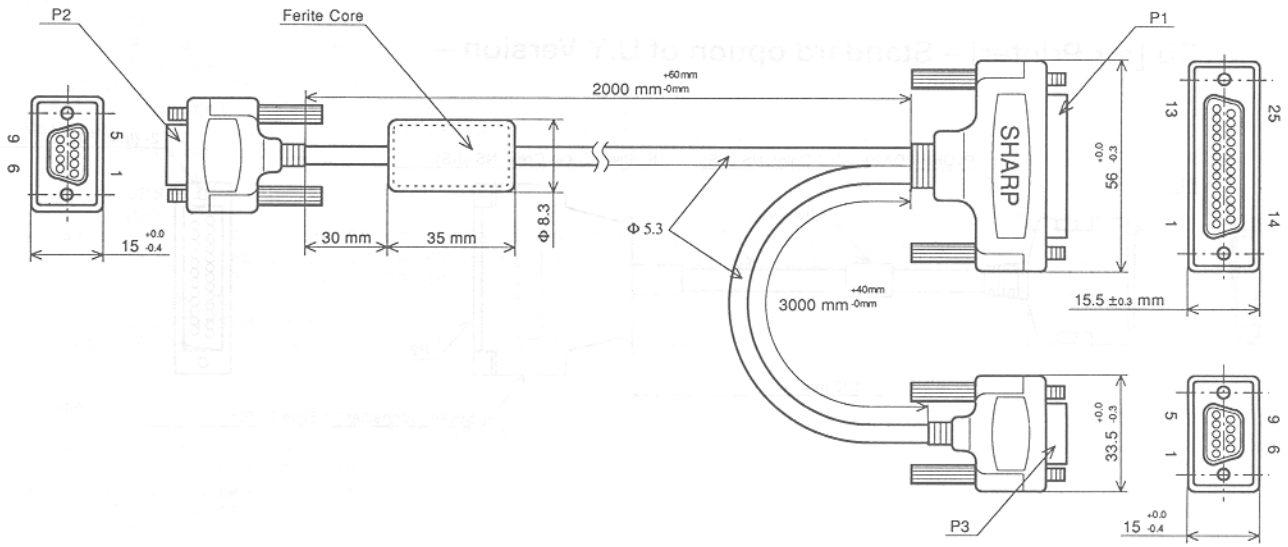
P1 [20pin]				P2 [25pin]			
1	$\overline{STB}$	11	BUSY	1	$\overline{STB}$	11	BUSY
2	D0	12	PE	2	D0	12	PE
3	D1	13	SEL	3	D1	13	SEL
4	D2	14	$\overline{AUTO}$	4	D2	14	$\overline{AUTO}$
5	D3	15	$\overline{ERROR}$	5	D3	15	$\overline{ERROR}$
6	D4	16	$\overline{INIT}$	6	D4	16	$\overline{INIT}$
7	D5	17	$\overline{SELIN}$	7	D5	17	$\overline{SELIN}$
8	D6	18	GND	8	D6	18	GND
9	D7	19	GND	9	D7	19	GND
10	$\overline{ACK}$	20	GND	10	$\overline{ACK}$	20	GND

2. CE-302CB [for RS-232-C] – Standard option of U.Y Version –



P1 [10pin]				9	25	P2	9-pin	25	
1	DCD	6	DSR	1	8	DCD	6	6	DSR
2	RX	7	RTS	2	3	RX	7	4	RTS
3	TX	8	CTS	3	2	TX	8	5	CTS
4	DTR	9	RI	4	20	DTR	9		RI
5	GND	10	(VCC)	5	7	GND			

3. CE-303CB [LAP LINK CABLE]



Materials:

- Cables: 7 Conductors, 26AWG, UL2464, Double Shield, Grey Color, Circle Diameter ϕ5.3mm – BFL.
- "D" Connector
  DB-25S-10 1pcs
  DB-09s-10 2pcs
  Phosphor Bronze with 10u Gold Plate on contact area.
- Thumber Screw: Grey Color – 6pcs.
- Aluminium Label with "SHARP" logo – 1pcs.
- Copper Foil (For shielding) – 6pcs.

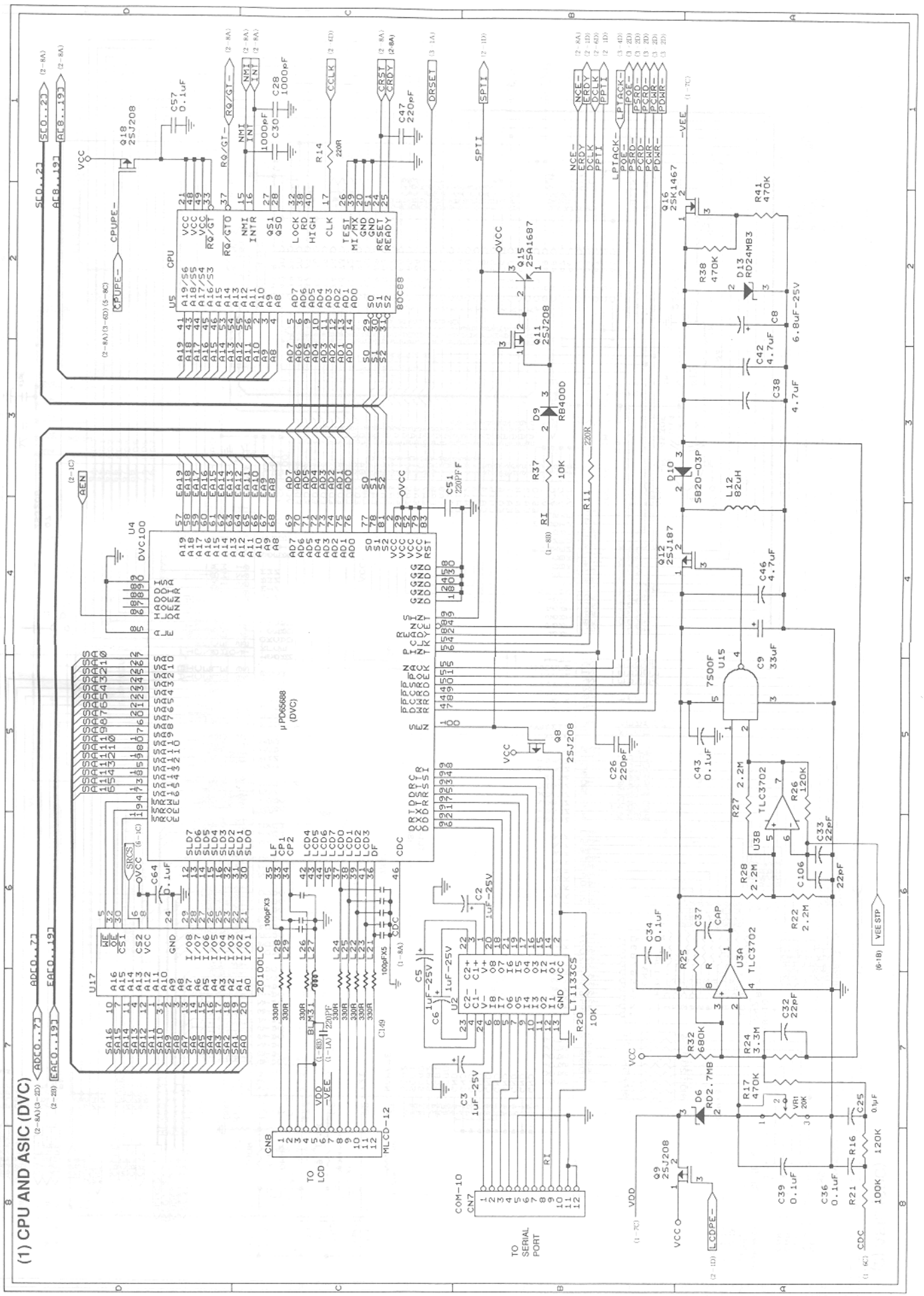
PIN CONNECTION TABLE

P2	P1	P3
DB-09S-10	DB-25S-10	DB-09S-10
PIN 2	PIN 2	PIN 3
PIN 3	PIN 3	PIN 2
PIN 8	PIN 4	PIN 7
PIN 7	PIN 5	PIN 8
PIN 4	PIN 6	PIN 6
PIN 5	PIN 7	PIN 5
PIN 6	PIN 20	PIN 4
SHIELD	SHIELD	SHIELD

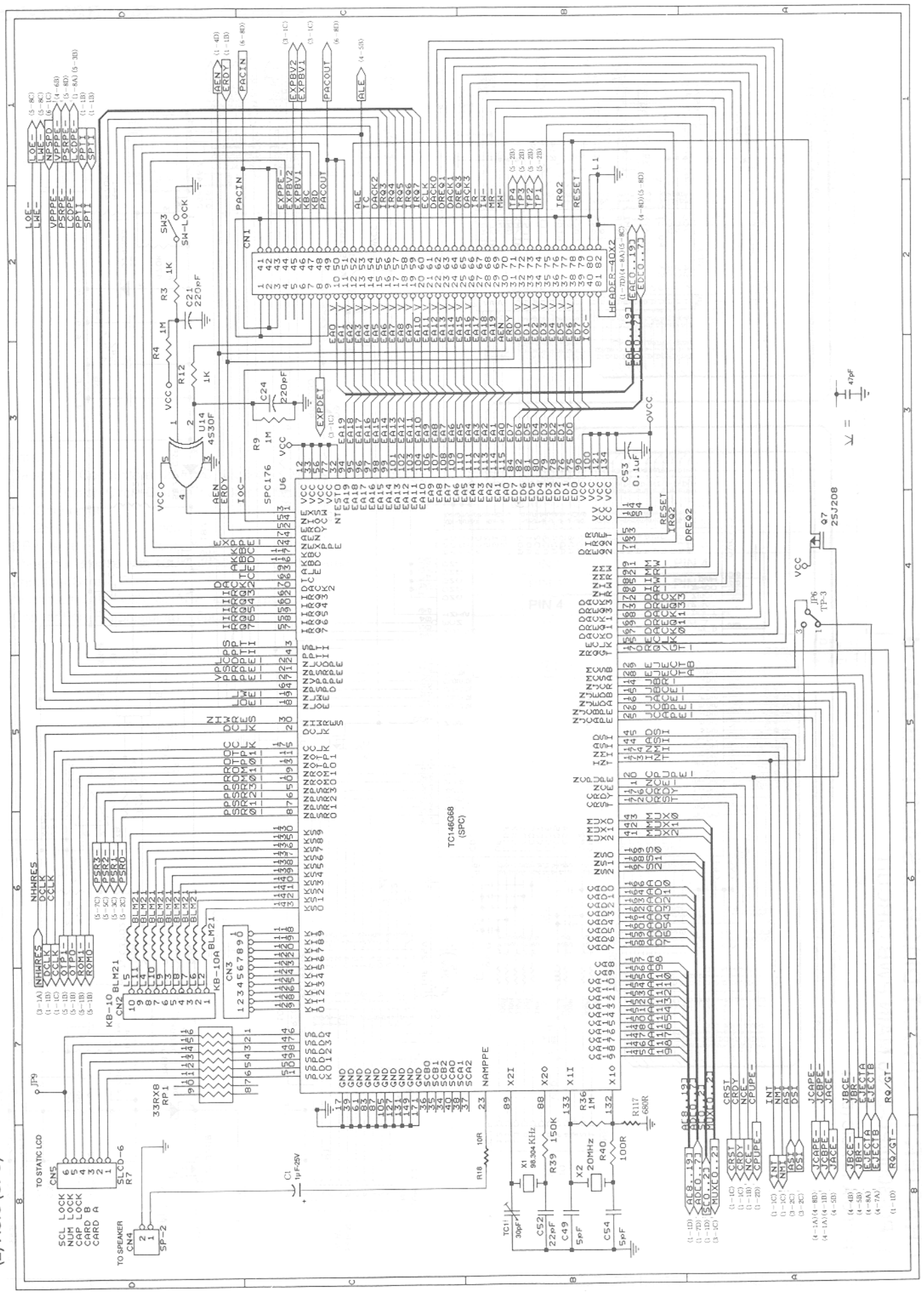
CHAPTER 12. CIRCUIT DIAGRAMS AND PWB LAYOUT

1. PC-3000/PC-3100 MAIN PWB CIRCUIT

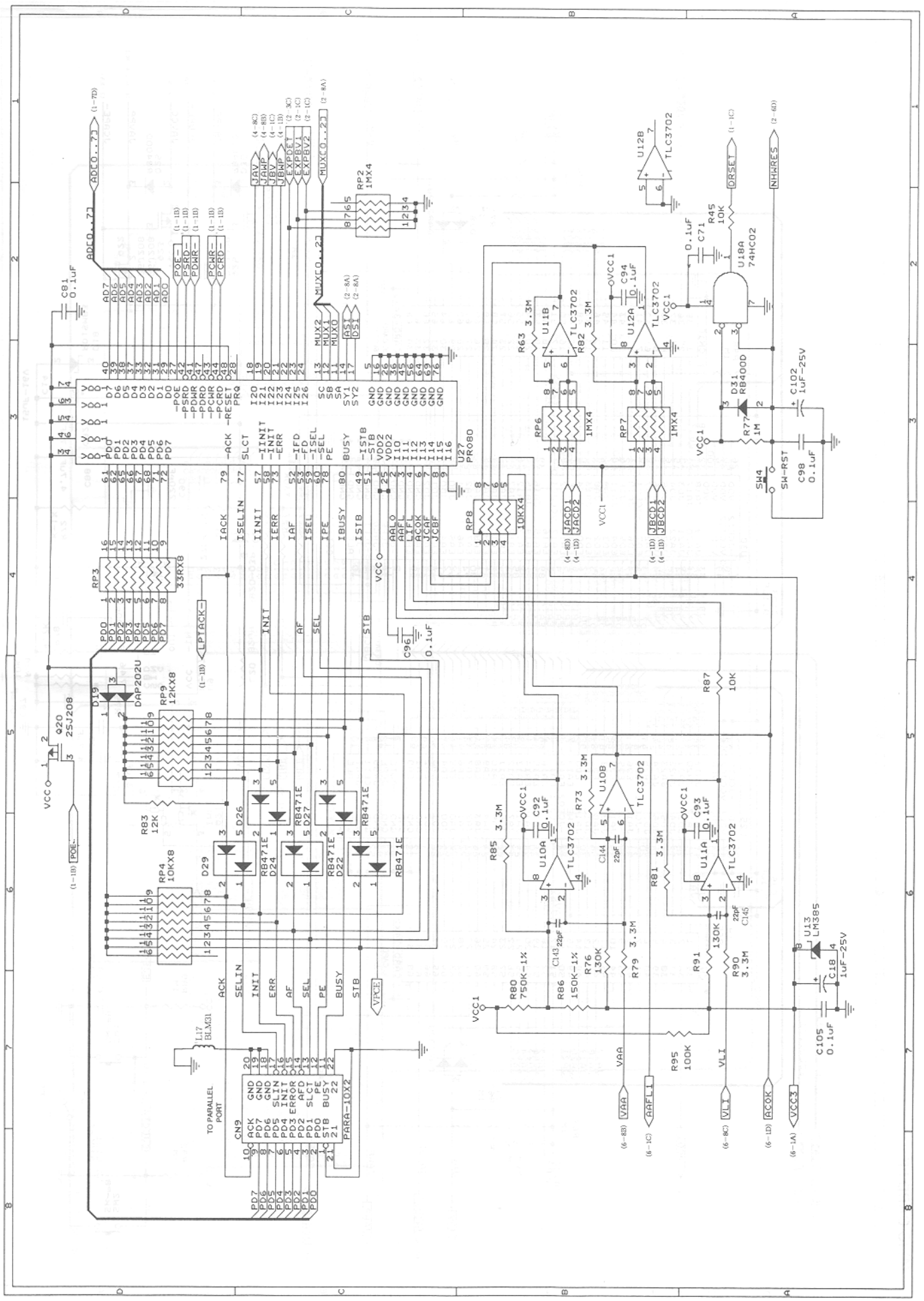
(1) CPU AND ASIC (DVC)



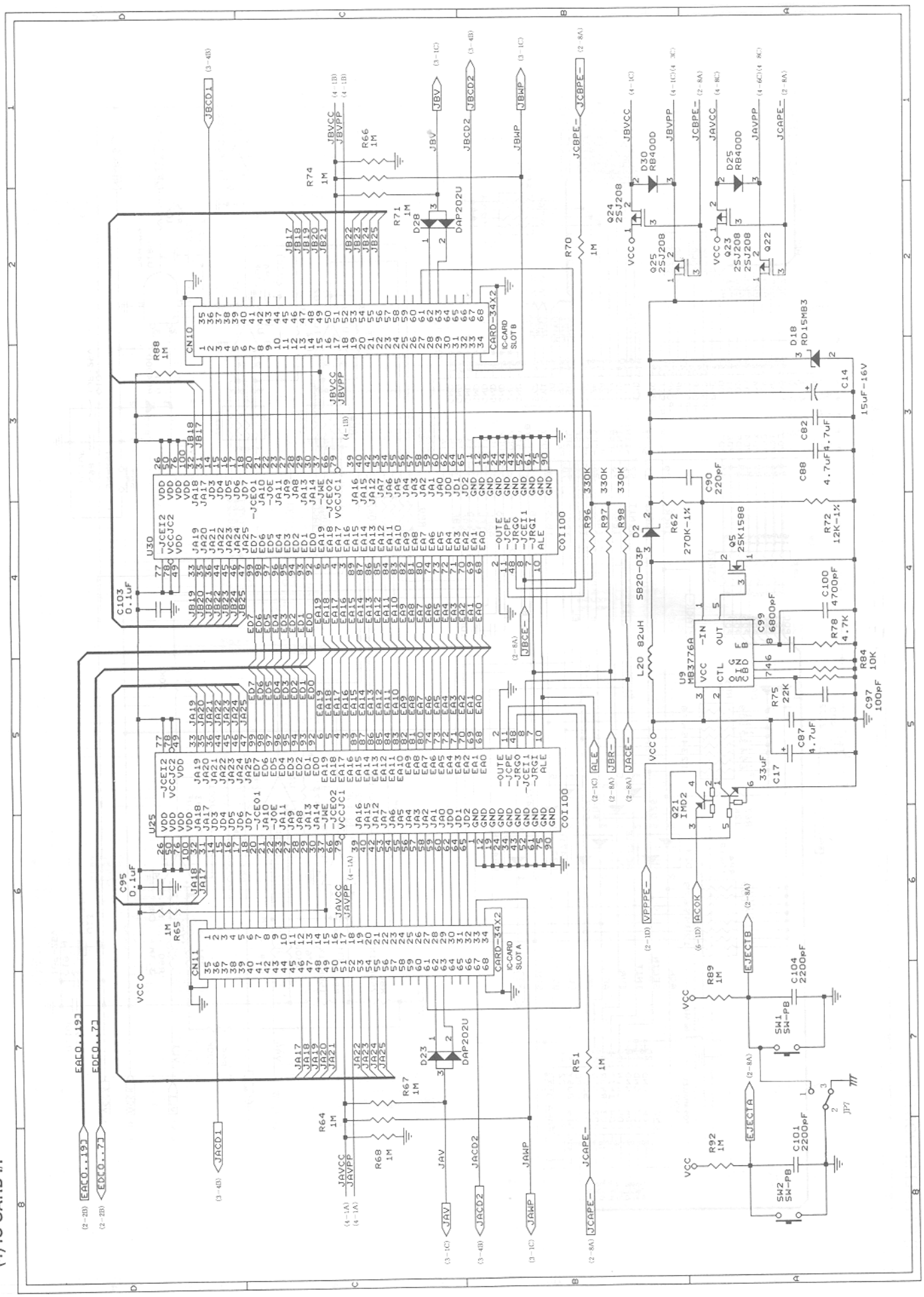
(2) ASIC (SPC)



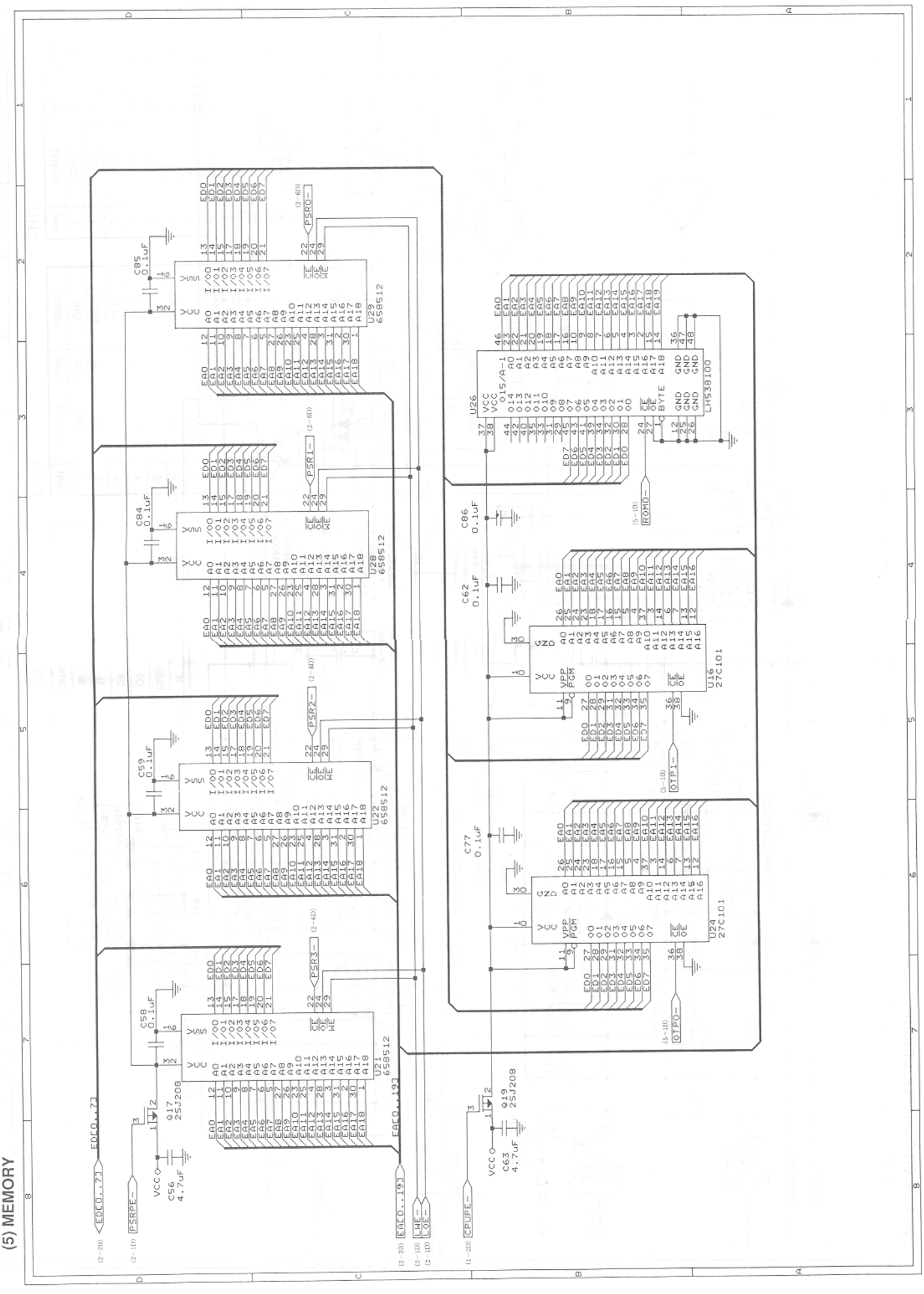
(3) PARALLEL PORT I/F



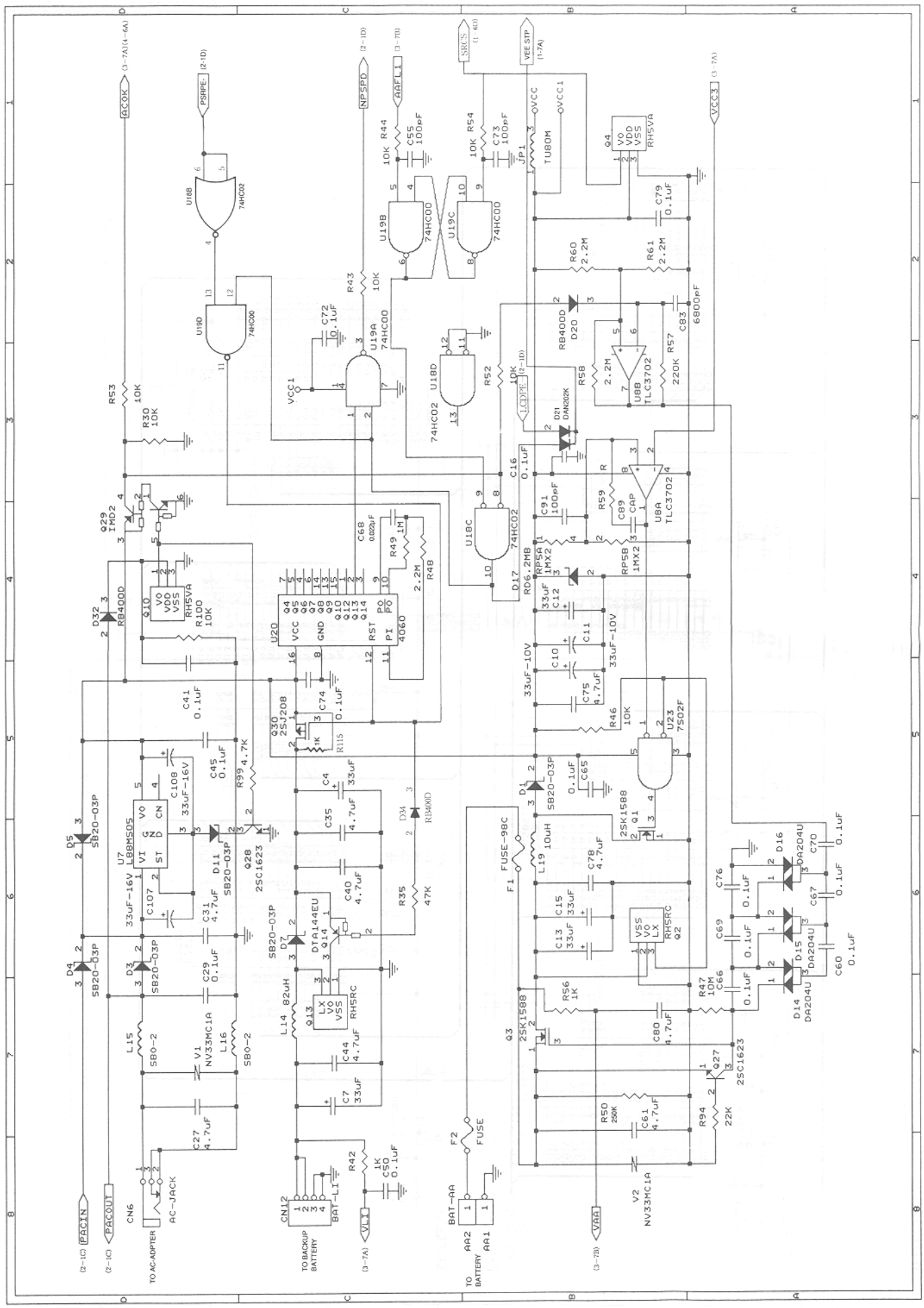
(4) IC CARD I/F



(5) MEMORY



(6) POWER CONTROL CIRCUIT



(7) PC-3000/3100 Main PWB Connector table

CN1

PIN	SIGNAL	PIN	SIGNAL
1	GND	41	GND
2	PACIN	42	PACIN
3	PACIN	43	PACIN
4	N.	44	_EXPPE
5	N.	45	_EXPBV2
6	N.	46	_EXPBV1
7		47	KBC
8	EXPDET	48	KBD
9	GND	49	PACOUT
10	EAO	50	PACOUT
11	EA1	51	PACOUT
12	EA2	52	
13	EA3	53	ALE
14	EA4	54	TC
15	EA5	55	DACK2
16	EA6	56	IRQ3
17	EA7	57	IRQ4
18	EA8	58	IRQ5
19	EA9	59	IRQ6
20	EA10	60	IRQ7
21	EA11	61	ECLK
22	EA12	62	DACK0
23	EA13	63	DREQ1
24	EA14	64	DACK1
25	EA15	65	DREQ3
26	EA16	66	DACK3
27	EA17	67	_IR
28	EA18	68	_IW
29	EA19	69	_MR
30	AEN	70	_MW
31	ERDY	71	TP1
32	ED0	72	TP2
33	ED1	73	TP3
34	ED2	74	TP4
35	ED3	75	DREQ2
36	ED4	76	GND
37	ED5	77	IRQ2
38	ED6	78	GND
39	ED7	79	RESET
40	_IOC	80	GND

CN2 KEY

PIN	SIGNAL	PIN	SIGNAL
1	KS0	6	KS5
2	KS1	7	KS6
3	KS2	8	KS7
4	KS3	9	KS8
5	KS4	10	KS9

CN3 KEY

PIN	SIGNAL	PIN	SIGNAL
1	KI0	6	KI5
2	KI1	7	KI6
3	KI2	8	KI7
4	KI3	9	KI8
5	KI4	10	KI9

CN4 SPEAKER

PIN	SIGNAL	PIN	SIGNAL
1	SOUND	2	GND

CN5 STATIC LCD

PIN	SIGNAL	PIN	SIGNAL
1	SPCK	4	CAP LOCK
2	CARD A	5	NUM LOCK
3	CARD B	6	SCL LOCK

CN6 AC-ADAPTER

PIN	SIGNAL	PIN	SIGNAL
1	ACD	3	ACG2
2	ASG1		

CN7 SERIAL PORT

PIN	SIGNAL	PIN	SIGNAL
1	I8	7	I3
2	I7	8	O2
3	O6	9	I1
4	O5	10	VCC
5	GND	11	GND
6	I4	12	GND

CN8 LCD

PIN	SIGNAL	PIN	SIGNAL
1	LF	7	_VEE
2	CP1	8	LCD0
3	GND	9	LCD1
4	CP2	10	LCD2
5	GND	11	LCD3
6	VDD	12	DF

CN9 PARALLEL PORT

PIN	SIGNAL	PIN	SIGNAL
1	STB	11	BUSY
2	PD0	12	PE
3	PD1	13	SLCT
4	PD2	14	AFD
5	PD3	15	ERROR
6	PD4	16	INIT
7	PD5	17	SLIN
8	PD6	18	GND
9	PD7	19	GND
10	ACK	20	GND

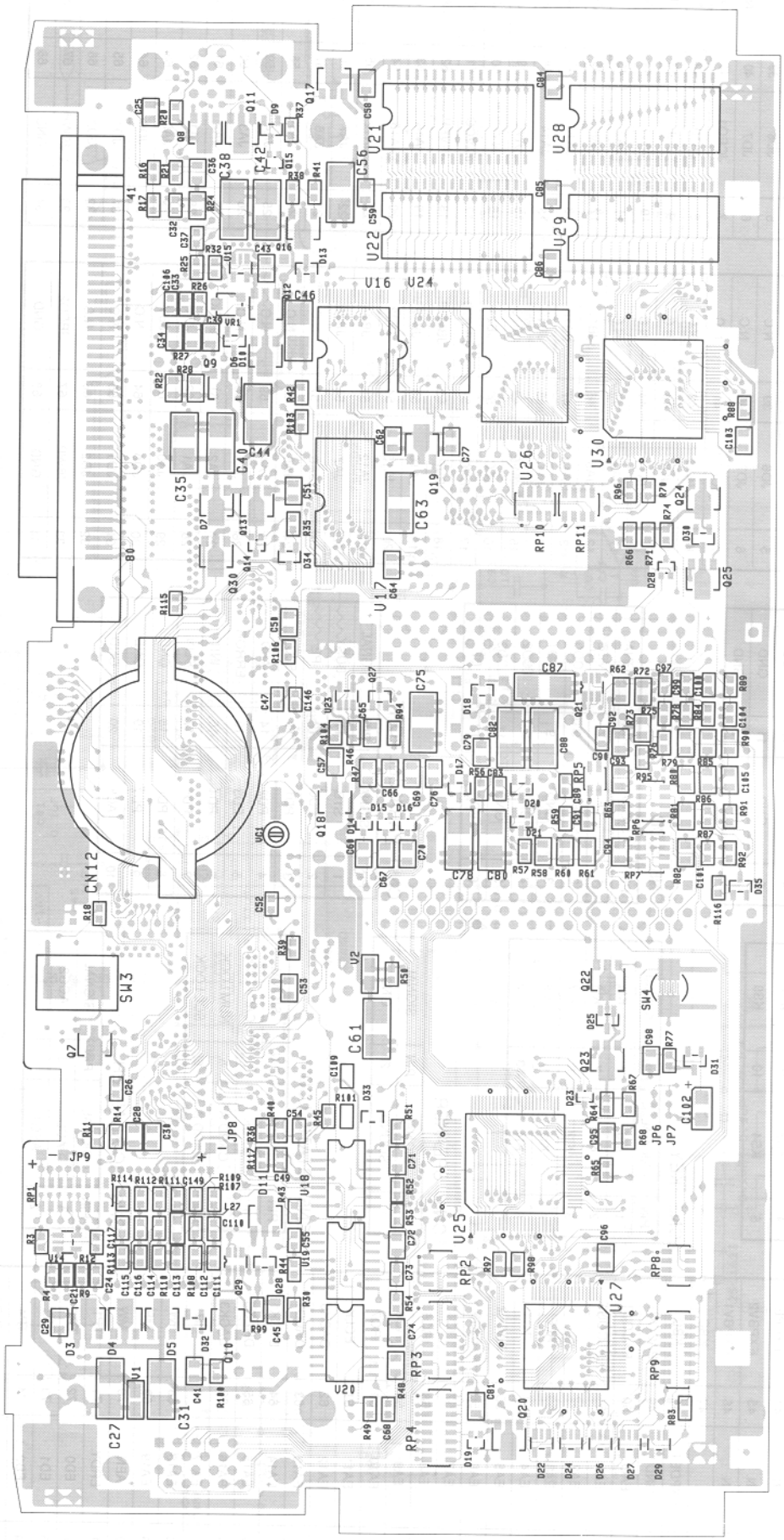
CN10

PIN	SIGNAL	PIN	SIGNAL
1	GND	35	GND
2	JD3	36	JBCD1
3	JD4	37	N.C
4	JD5	38	N.C
5	JD6	39	N.C
6	JD7	40	N.C
7	_JCEO1	41	N.C
8	JA10	42	N.C
9	_JOE	43	N.C
10	JA11	44	N.C
11	JA9	45	N.C
12	JA8	46	JB17
13	JA13	47	JB18
14	JA14	48	JB19
15	_JWE	49	JB20
16	N.C	50	JB21
17	JBVCC	51	JBVCC
18	JBVPP	52	JBVPP
19	JA16	53	JB22
20	JA15	54	JB23
21	JA12	55	JB24
22	JA7	56	JB25
23	JA6	57	N.C
24	JA5	58	N.C
25	JA4	59	N.C
26	JA3	60	N.C
27	JA2	61	_JRGO
28	JA1	62	JBV
29	JA0	63	JBV
30	JD0	64	N.C
31	JD1	65	N.C
32	JD2	66	N.C
33	JBWP	67	JBCD2
34	GND	68	GND

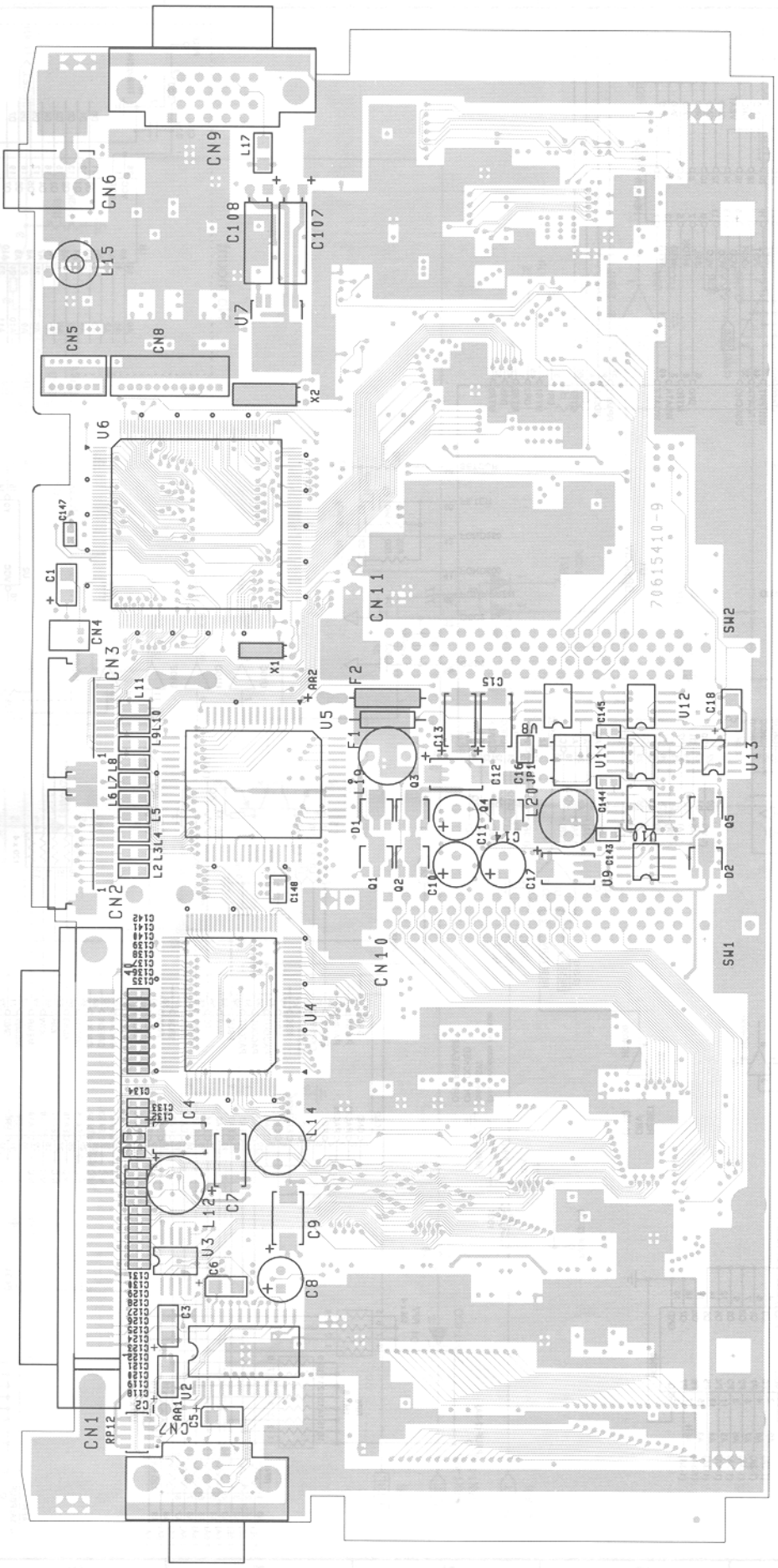
CN11

PIN	SIGNAL	PIN	SIGNAL
1	GND	35	GND
2	JD3	36	JACD1
3	JD4	37	N.C
4	JD5	38	N.C
5	JD6	39	N.C
6	JD7	40	N.C
7	_JCEO1	41	N.C
8	JA10	42	N.C
9	_JOE	43	N.C
10	JA11	44	N.C
11	JA9	45	N.C
12	JA8	46	JA17
13	JA13	47	JA18
14	JA14	48	JA19
15	_JWE	49	JA20
16	N.C	50	JA21
17	JAVCC	51	JAVCC
18	JAVPP	52	JAVPP
19	JA16	53	JA22
20	JA15	54	JA23
21	JA12	55	JA24
22	JA7	56	JA25
23	JA6	57	N.C
24	JA5	58	N.C
25	JA4	59	N.C
26	JA3	60	N.C
27	JA2	61	_JRGO
28	JA1	62	JAV
29	JA0	63	JAV
30	JD0	64	N.C
31	JD1	65	N.C
32	JD2	66	N.C
33	JAWP	67	JACD2
34	GND	68	GND

(9) PC-3000/3100 MAIN PWB LAYOUT (BOTTOM VIEW)



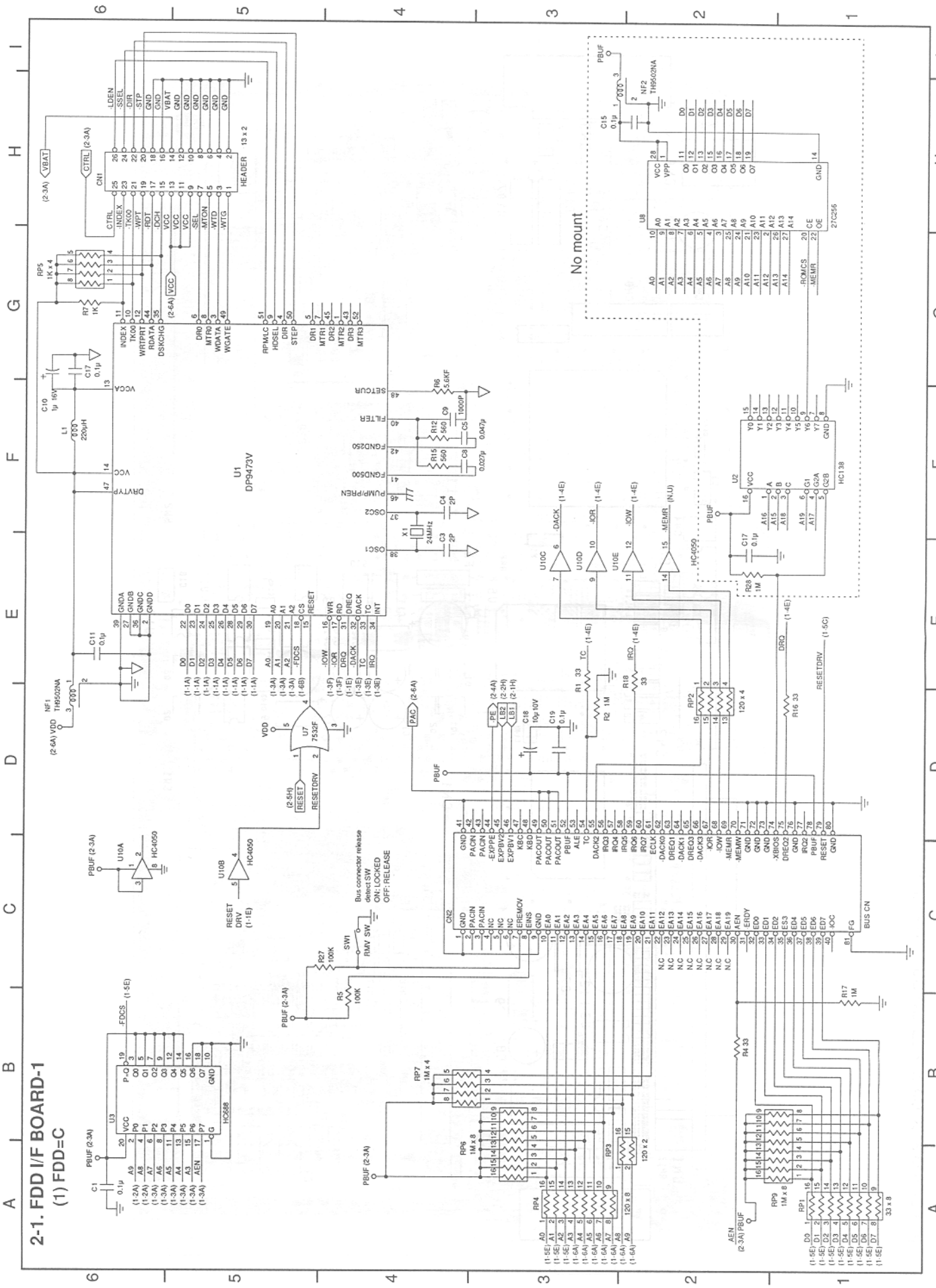
(8) PC-3000/3100 MAIN PWB LAYOUT (TOP VIEW)



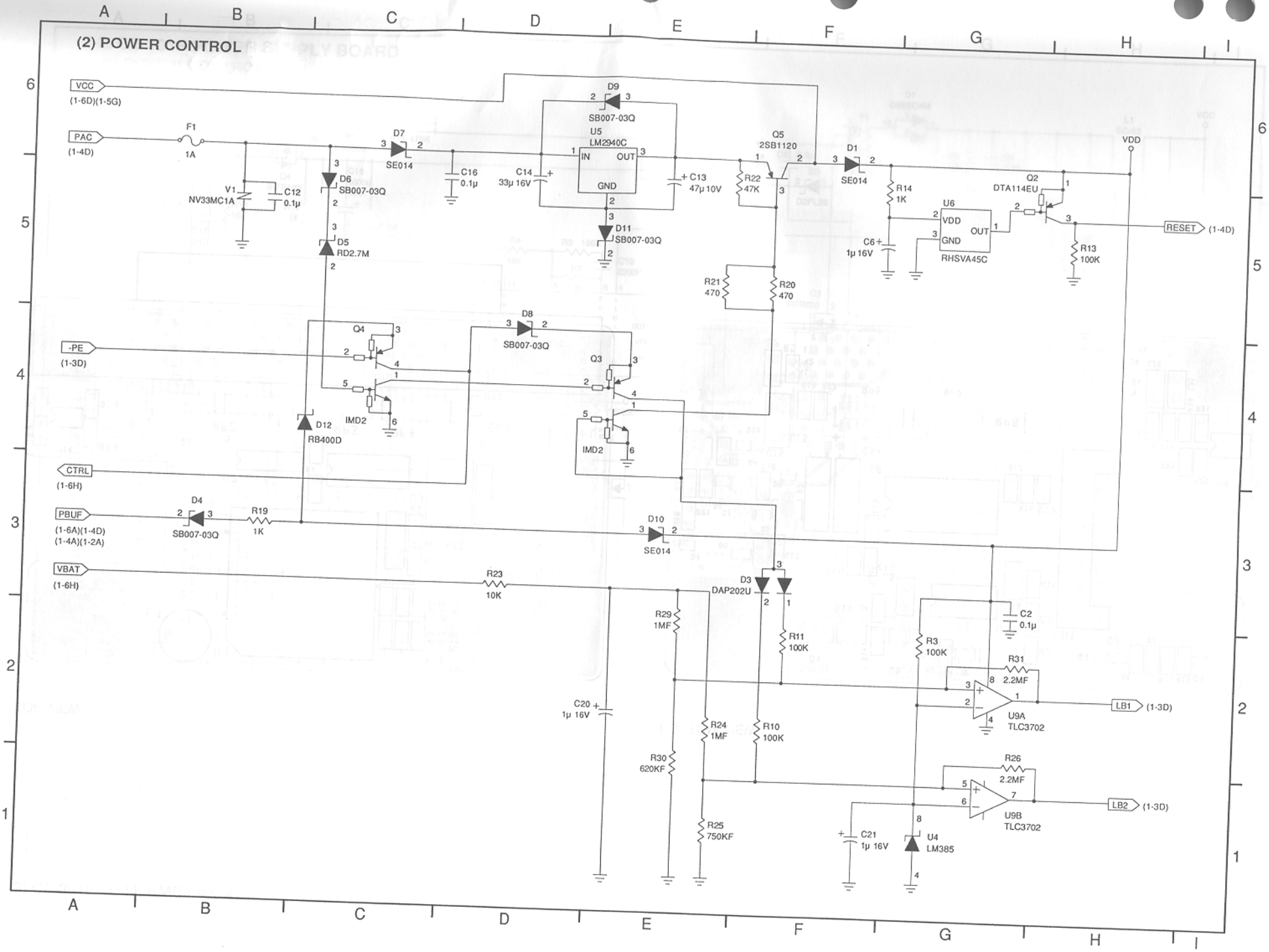
2. CE-301F (FDD UNIT) CIRCUIT

2-1. FDD I/F BOARD-1

(1) FDD=C

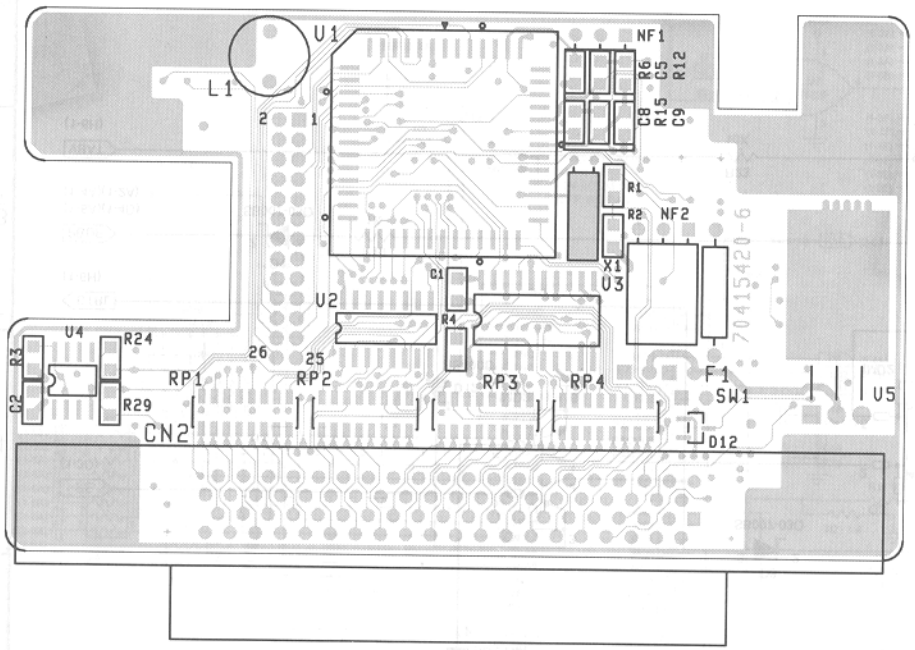


(2) POWER CONTROL

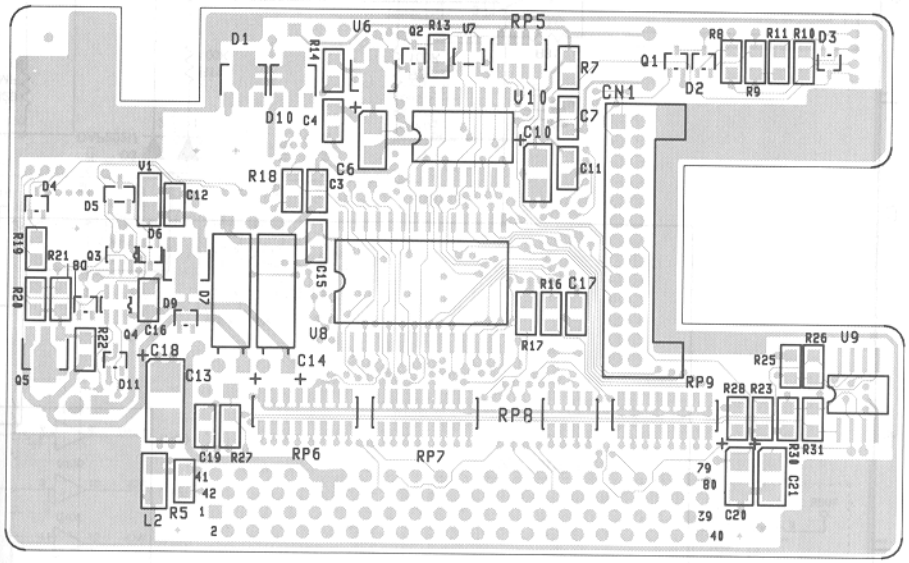


(3) CE-301F FD I/F PWB LAYOUT

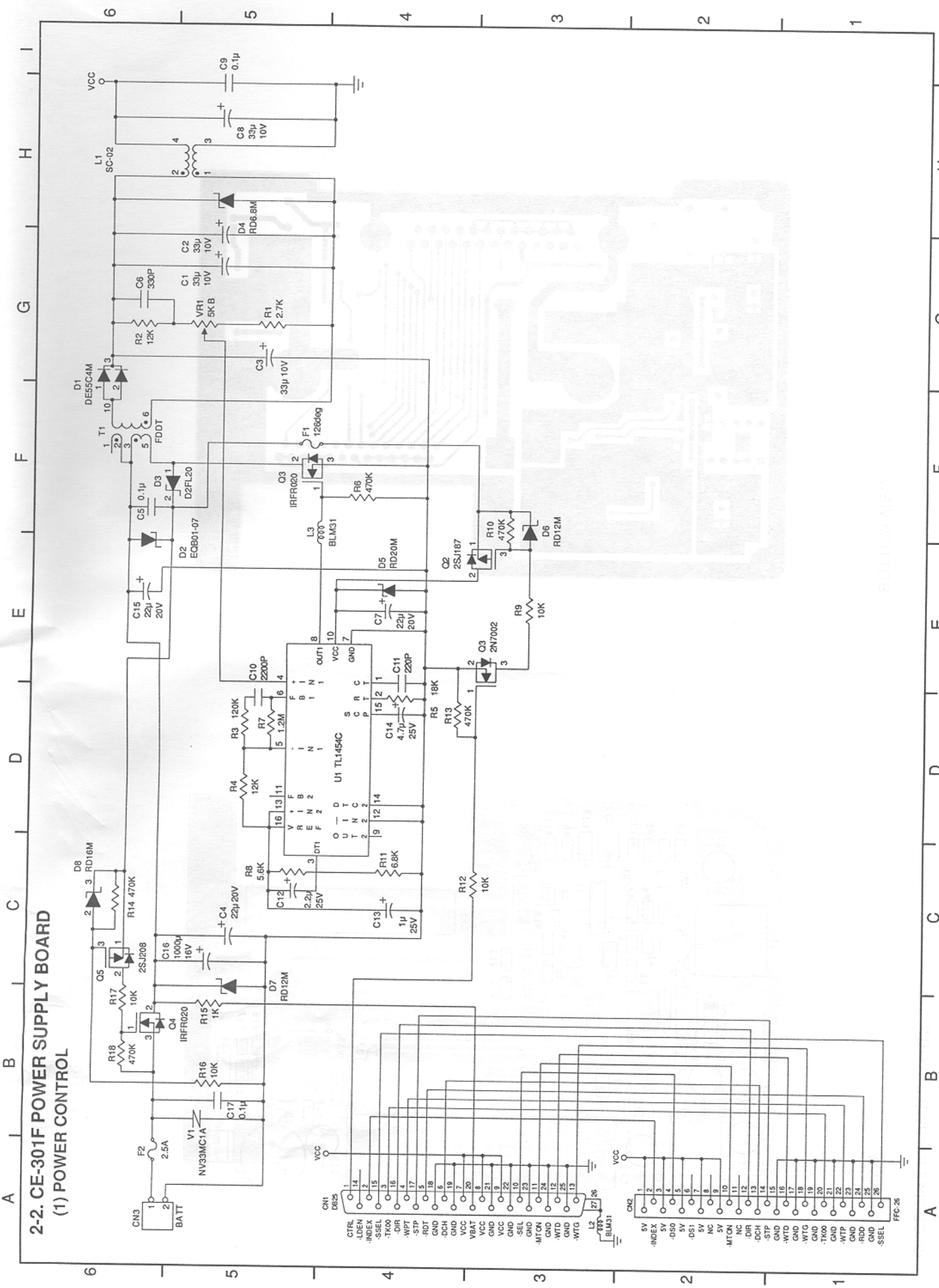
TOP VIEW



BOTTOM VIEW

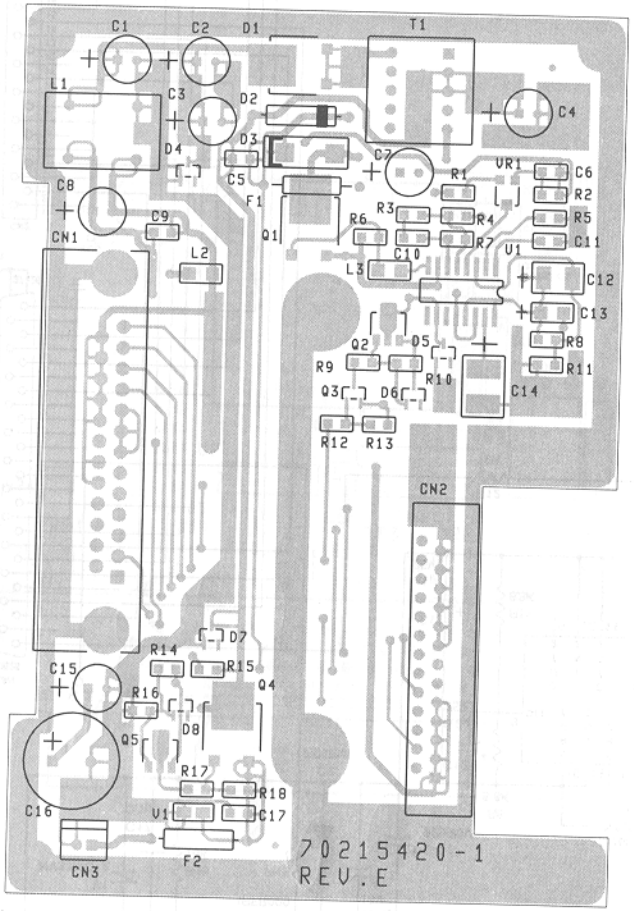


2-2. CE-301F POWER SUPPLY BOARD
(1) POWER CONTROL



(2) CE-301F P/S PWB LAYOUT

TOP VIEW



BOTTOM VIEW